Philips DVDR75

Technical Training Manual

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PHILIPS

Introduction

This manual is intended for use by the Service Technician. There are two versions of the DVDR75. The first four digits of the Product Number indicates the version. The Product Number is similar to a Serial Number. It will read VN02 or VN04. The VN04 is the newer of the two. The VN04 uses an updated Digital Board that contains the functionality of the DVIO Board. When there are two versions of a circuit, the title to the section will have one or the other in the title, VN02 or VN04.

The first portion of this manual contains a basic description of disc based data playback and recording technologies. Self Diagnostics are included to aid in troubleshooting. Technical Descriptions of the circuitry are followed by a Troubleshooting Section.

The DVDR75 is the forth generation in a line of DVD recorders. Recordings can be made from broadcast transmissions, and from other analog or digital sources. The DVDRW format allows the user to record and erase a disc many times. The recorded discs will play on most existing and future DVD players. The DVDR75 has a connection for DV or Digital camcorders via an I-Link or Firewire connection. This connection technically is called an IEEE 1394 connection. This machine records on 4.7Gbyte DVD+R and DVD+RW discs. This machine uses a real-time MPEG2 Variable Bit Rate, VBR, Video encoder. The DVDR75 plays back DVD Video, Video CD, Audio CD, CD-R, and CD-RW discs.

Its many features include: Favorite Scene Selection for easy editing, Index Picture Screen for instant overview of contents, Digital Time Base Corrector, Digital Audio output (DTS, AC-3, MPEG, PCM), TruSurround for 3D sound, Zoom + Perfect Still. It is Widescreen, 16:9 compatible, and has a Universal Remote Control, 20 disc resume, Disc Lock, and One Touch Recording.

Virgin Mode

The DVDR75, when first hooked up, needs to get information from the user about what language and what local broadcast system the unit is going to operate with. Use the remote to make those selections. The unit will not operate until this process is completed. If you want the recorder to start up in Virgin mode, unplug the recorder. Plug the recorder in again while holding the STANDBY-ON button.

DVD Basics

Philips with nine other manufacturers chose a format specification for DVDR and RW on March 16, 2001. This format uses Real Time recording. Its recording is compatible with DVD-Video, and DVD ROM. The data blocks use lossless linking. The physical layout matches very closely to that of a DVD ROM. See **Figure 1**. It also uses Direct Overwrite when a RW disc is used.

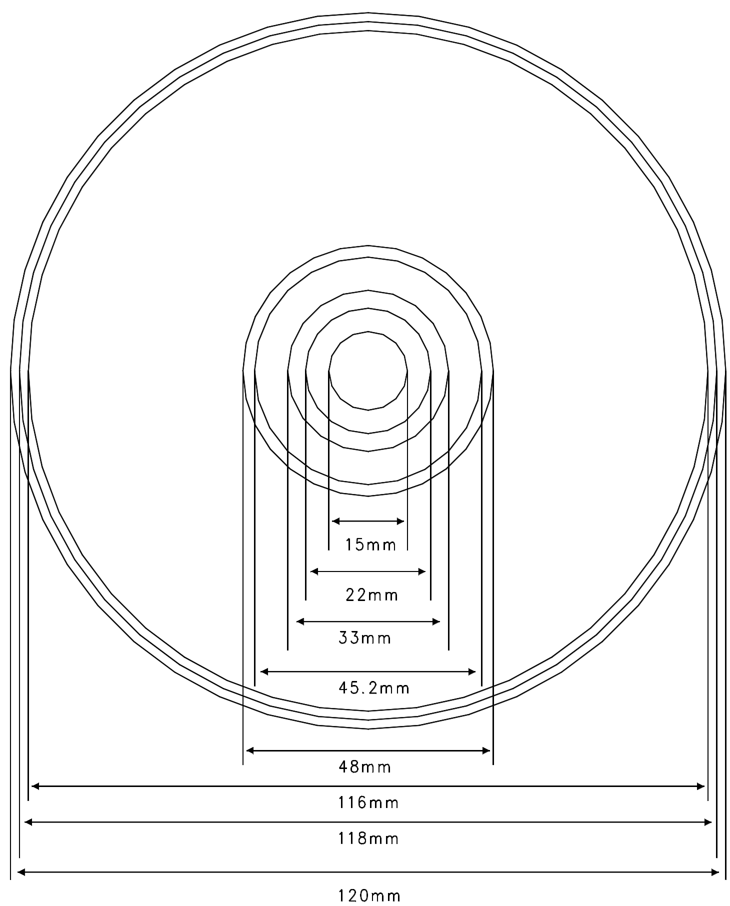


Figure 1 – DVD ROM Disc

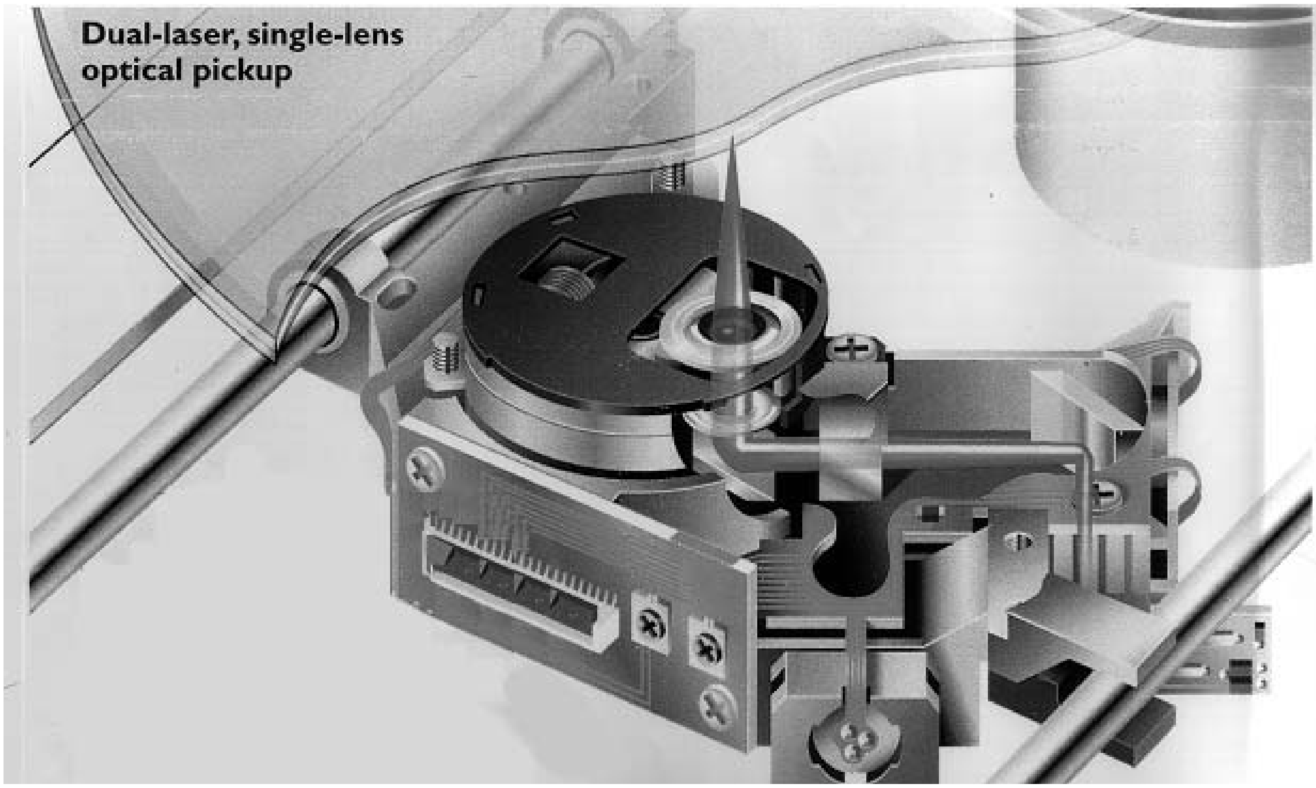


Figure 2 – CD Laser Operation

Laser Technology

The DVD and CD share much of their technology. We will start with CDs and work our way to the DVD. CDs use a red laser created by a diode and lens system often called a Light Pen. Refer to **Figure 2**. The narrow beam of light is focused onto the reflective layer of a disc. At the instant that focus is achieved, the disc is spun. The laser starts on the innermost tracks of the CD and reads outward. At the beginning of the disc is the Table of Contents. At the bottom of the Light Pen are Monitoring Diodes. The Monitoring Diodes provide information about focus and tracking. Data is retrieved from the disc in the form of pulses of light reflecting from the disc. The pulses are created by Pits in the Reflective Layer of the disc. The Pits reflect less light than the intact surface of the Reflective Layer, called Lands. The data is binary. A 1 is generated when the light transitions from bright to dim and dim to bright. The time between is a series of zeros determined by the data rate.

Disc Mechanical Layout

The CD is a plastic disc 120mm in diameter, with a thickness of 1.2mm. **Refer to Figure 3**. It has a silver colored Reflective Layer. The maximum playing time for a music recording on a Compact Disc, CD, is 74 Min.

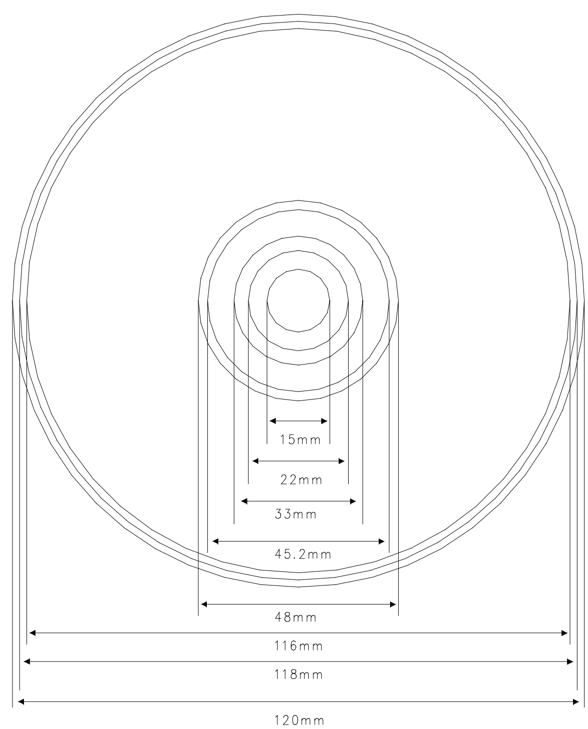


Figure 3 - CD Disc

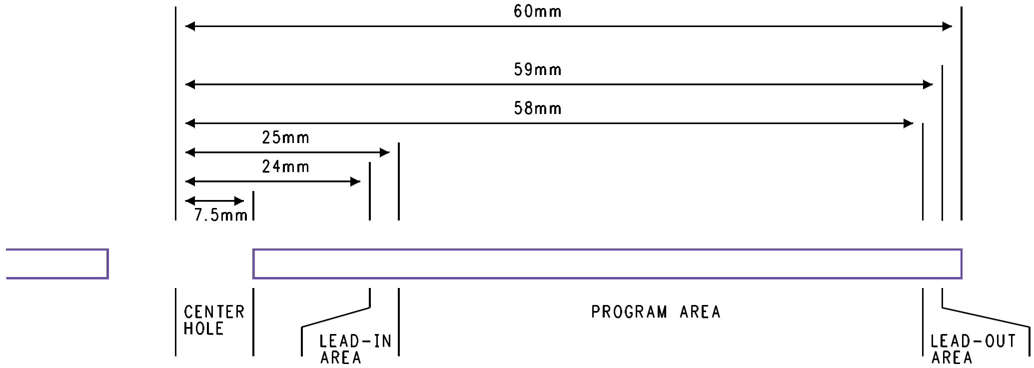


Figure 4 - The Disc

The CD is less vulnerable to damage than an analog record. That does not mean it does not have to be treated with care. Dirt and heavy scratches can interfere with playability.

As shown in **Figure 4**, the CD is subdivided into three parts: the Lead In Track, the Program Area, and the Lead Out Area. These three sections together are considered the Information Area. There is a hole in the center for holding the disc. The disc is held between two equally sized concentric rings. The rings have an inner diameter of 29mm and an outer diameter of 31mm.

The Data on the disc is recorded on a spiral shaped track with pits and lands. The reflective side of the disc contains the tracks.

The production of a disc is a high tech process explained in **Figure 5**. The process starts with glass that is photo etched. The glass is silver plated and is used as a form for a metal cast. The metal cast is used to stamp a nickel Mother Stencil. The Mother Stencil is used to stamp the Son Stencil. Son Stencils are used to stamp the foil of the discs. A protective layer and label are added.

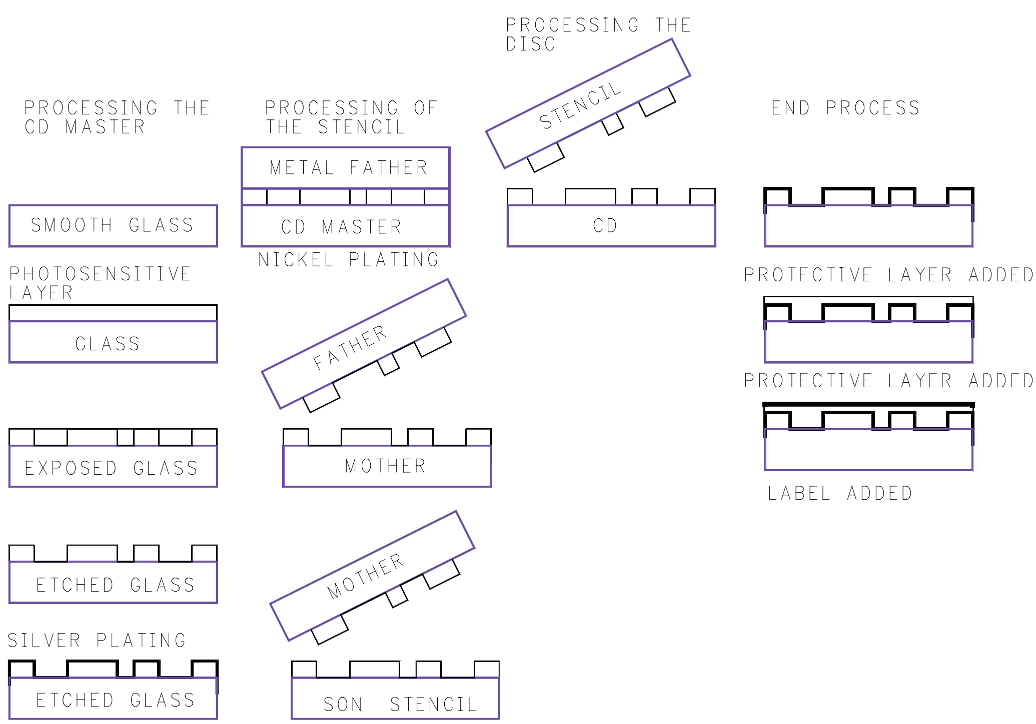


Figure 5 - Creating a CD

Read Process
The Servo circuit is responsible for focusing the laser and moving the Light Pen to follow the spiraling tracks on the rotating disc. The digital High Frequency information, HF, is demodulated and stored in RAM. When the RAM is half full, the data is fed out to the Digital to Analog Converters. The speed of the rotating disc is servo controlled to keep the RAM half full. The analog signals are amplified and sent to the output connectors.

Record Once Technology

Disc Mechanical Layout
From an external point of view, a DVD is the same as the CD. Recordable media creates the need for three physical layouts. There are three possible states of a disc: a blank disc, a partially recorded disc, and a full or finalized disc. The difference is in the way the Information Area is divided. The Information Area of a blank disc extends from 22.35 mm centered on the disc to 59 mm centered on the disc. Refer to **Figure 6.** A partially recorded disc's Information Area has four sections: a PCA/RMA area, a Lead In Area, a Recorded Program Area, and a Recordable Program Area. See **Figure 6** for the dimensions. The PCA Area is the Power Calibration Area, PCA. The RMA Area is the Recording Management Area. A fully recorded or finalized disc's Information Area has three sections: A lead in Area, the Program Area, and the Lead Out Area. See **Figure 7** for the dimensions.

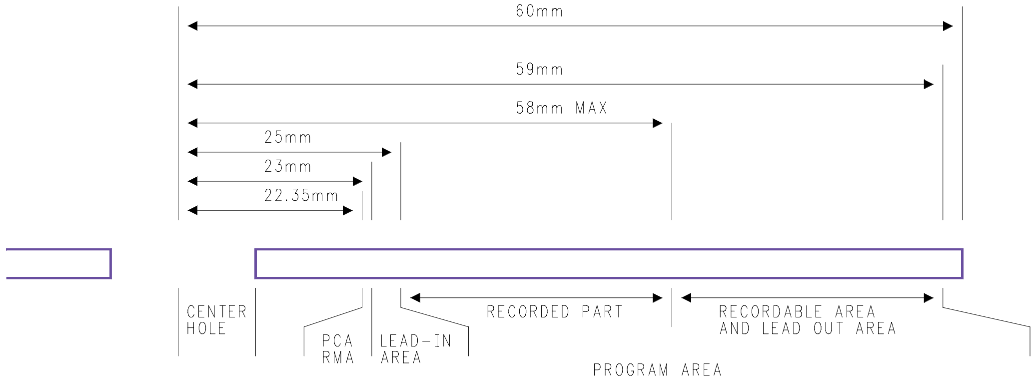


Figure 6 – A Partially Recorded Disc.

The disc's recordable layer contains major differences from that of a stamped disc. The blank disc has a Pre-groove stamped into the recordable layer of the disc. This is polycarbonant for DVD+Rs and organic dye material for DVD+RWs. This spiral Pre-groove is for the Servo circuit to provide a mechanical reference during recording. The dye based RW recordable layer provides a reflectivity of 40% light return and 70% light return. 40 percent reflectivity represents Pits and the 70% represent the Lands.

Record Process
The record process shares most of its mechani-

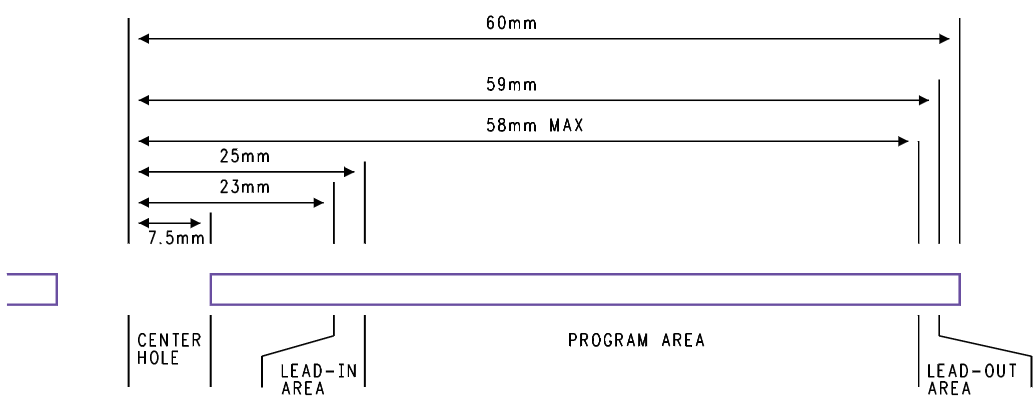


Figure 7 – Fully Recorded or Finalized Disc

cal operation with that of the play process. The main difference is how the Servo is locked to the disc. The Servo follows the Pre-groove for Radial Tracking and disc speed. The speed of the disc is locked to a wobble signal that is part of the spiral grove stamped into the disc.

The intensity of the laser beam is modulated from playback intensity to write intensity. As the disc reads the Pre-groove, the laser arrives at a position where a Pit is to be formed. The laser power increases from 4mW to 11mW. This raises the temperature of the disc to 250 degrees Celsius. The recordable layer melts, reducing its volume. The polycarbonate flows into the space vacated by the dye. The modulation from read laser power to write laser power forms a pit and land pattern effectively the same as a prerecorded disc.

Re-recordable Technology

Disc Mechanical Layout

Disc usage mechanically is identical to the recordable media. The only difference is the chemical make up of the recordable layer. The recordable layer is made up of an alloy of silver, indium, antimony and tellurium.

Re-Recording Process

The Re-Record process shares much of its operation with that of a CDR. The blank disc's Information Area is in a polycrystalline state. During recording, the laser power is modulated from 8mW to 14mW. 8mW is the playback laser power and 14mW is the record laser power. The polycrystalline state of the recordable surface changes, or melts at 500-700 degrees C into an amorphous state. The melted, amorphous areas reflect light less than the crystalline areas, creating a pattern similar to the stamped CD. A major difference of CDRWs from CDRs is the ability to erase.

The Erase Process

To Erase a CDRW disc, the recordable layer must be returned to its polycrystalline state. This is done by heating up the temperature of the recorded surface to 200 degrees C. This is less than the melting point. This is done at X2 recording speed. The slower speed allows time for the alloy to return to its proper state. This takes approximately 37 min. Some software erases the just the TOC on the disc and allows the disc to be rewritten. This method is not as reliable

Over Writing Process

Over writing combines the processes of erasing and writing. When the disc and Light Pen are in position to start writing the new data, the laser power starts modulating in the same manner as it does for normal recording with one difference. During the time there is to be a land, the laser power goes to the erase level rather than the playback level.

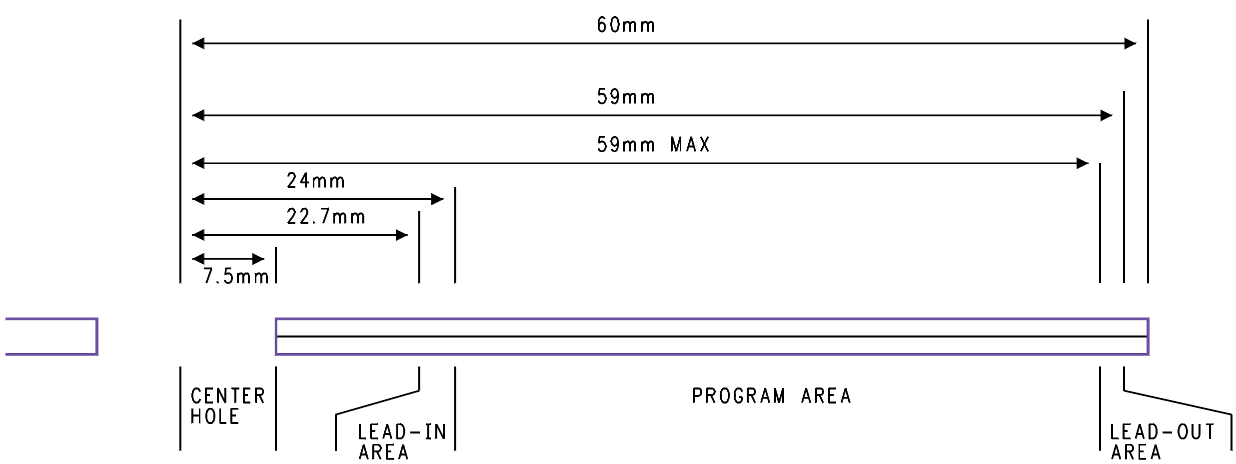


Figure 8 – Mechanical Layout of a DVD

DVDs

All of the previously discussed technologies apply to the DVD. Like CDs, DVDs are also stamped into play only discs. In this discussion, we will point out the differences between DVDs and CDs. If you are new to disc based technology, you will want to start with the information preceding this discussion.

mm centered. The Lead In Area is smaller, measuring 22.7 mm centered to 24 mm centered. The Information Area is limited to 116mm centered.

Two of the big differences between DVDs and CDs are the Pit and Land sizes, and the track widths. Refer to **Figure 9.**

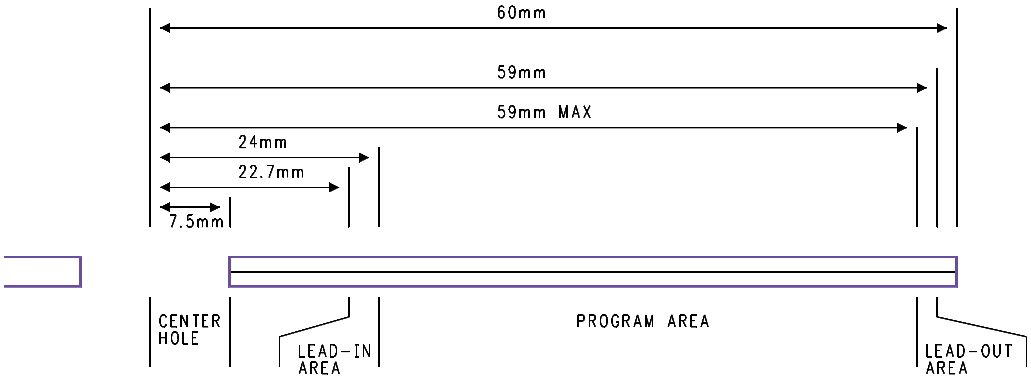


Figure 8 - DVD Mechanical Layout

DVD Disc Mechanical Differences

Most DVDs are single sided, however, the DVD specification allows for two readable layers, and the disc can be double sided. We will start our discussion with single sided, single layered discs. A Digital Versatile Disc, DVD, looks very similar to a CD. Refer to **Figure 8**. The Clamping Area is larger, starting at 11 mm centered to 16.5

The Manufacturing process of a DVD is comparable to that of a CD. The main difference is the thickness. The DVD can be a double sided product. Each side is .6mm. The two sides are glued back to back, producing 1.2mm total thickness.

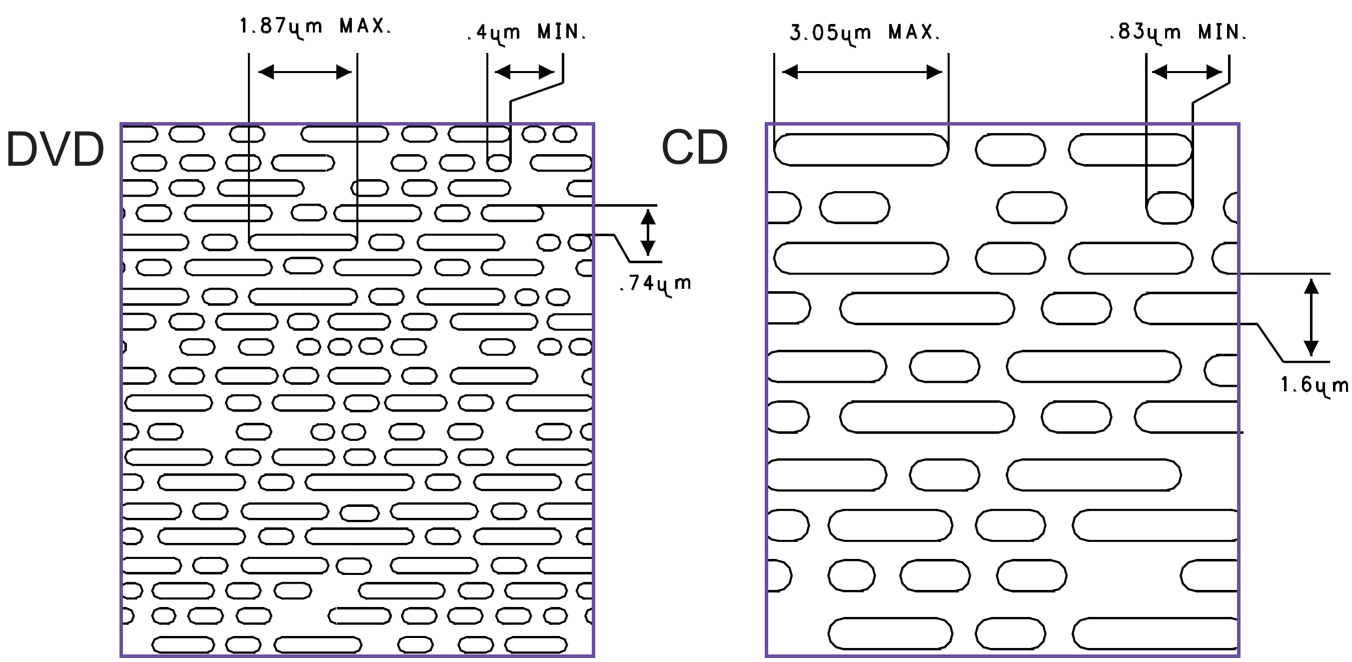


Figure 9 – DVD and CD Pit Structure.

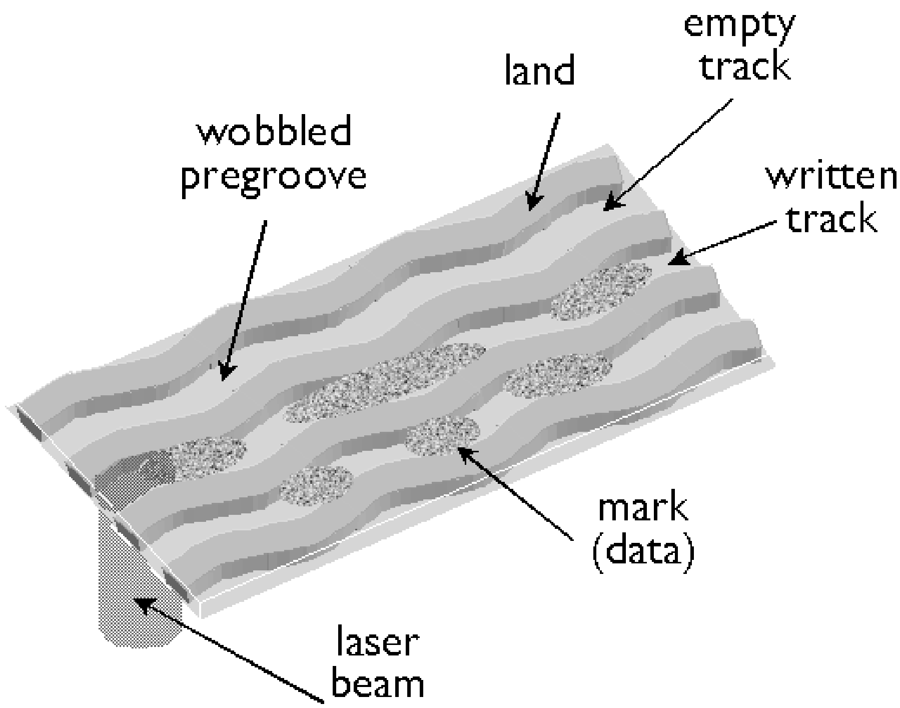


Figure 10 - Wobble Pregroove

Wobble

A Pre-groove is stamped on writable discs.
All recordable DVD media types feature a microscopic wobble groove embedded in the plastic substrate. This wobble provides the recorder with the timing information needed to place the data accurately on the disc. During recording, the drive's laser follows this groove, to ensure consistent spacing of data in a spiral track. The walls of the groove are modulated in a consistent sinusoidal pattern so that a drive can read and compare it to an oscillator for precise rotation of the disc. This modulated pattern is called a wobble groove because the walls of the groove appear to wobble from side to side. This signal is only used during recording, and therefore has no effect on the playback process. Among the DVD family of formats, only recordable media use wobble grooves.

Dual Layer Discs
Two information layers are separated by a thin transparent layer. Refer to **Figure 11**. The first layer is partially transparent. This allows the second layer to be read through the first layer. Both layers are read by controlling the focus. There are two methods for reading the data of a Dual Layer disc, PTP and OTP. Refer to **Figure 12**.

PTP is Parallel Track Path. That means the Lead In and Out Areas of the two layers correspond to each other. Each Lead In Area is on the inner portion of the disc, and the Lead Out Area is on the outer portion of the disc. This is useful to link data between the layers.

This allows instant access to the additional data or scene. OTP is Opposite Track Path. This method links the end of one layer to the beginning of the other. The Lead In Area is still on the

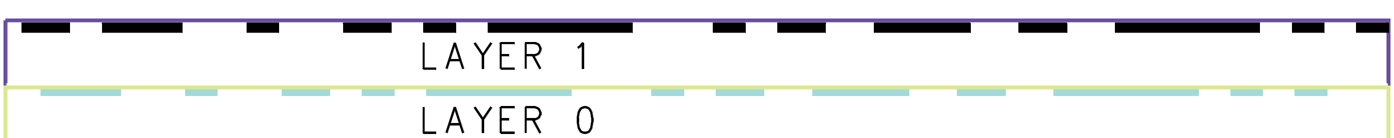


Figure 11 – Dual Layer DVD

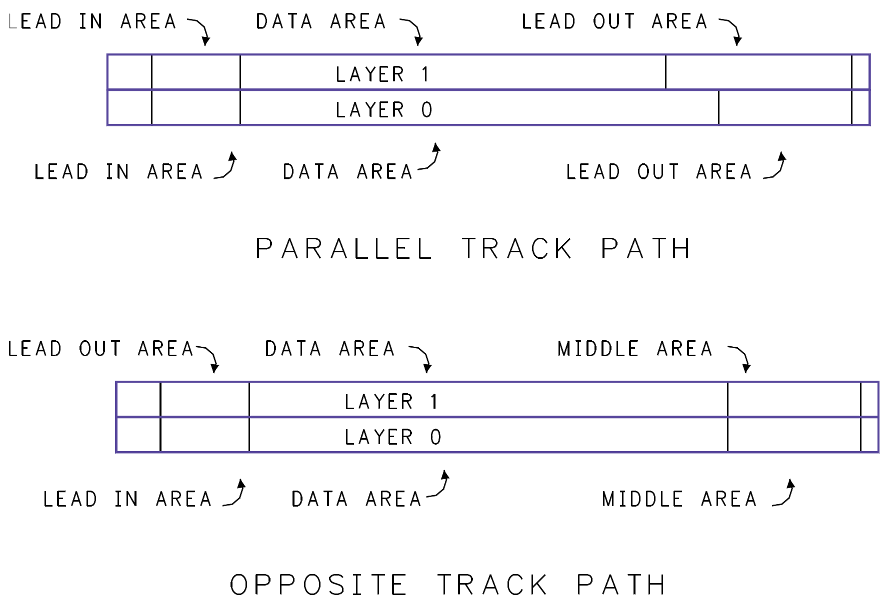


Figure 12 – PTP and OTP Layout

inner portion of the disc. There is a Middle Track Area on both of the layers located on the outer portion of the layers. The Middle Track Area links the data on the two layers together. The Lead Out Area is on the second layer on the inner portion of the disc.

Capacity

Because a stamped DVD can be Dual Layered and Double Sided, there are four different capacities. Refer to **Figure 13**. These capacities strictly pertain to raw data. The time available for Video and Audio has many extra factors that determine the length of time on each side or layer. The picture complexity and the amount of movement in the picture affect compression and time on a disc. The number of languages affect the time on a disc. The type and quality of the Audio has an affect on the time also. It can be mono, stereo, or AC-3. Therefore, the media itself determines the capacity in time on the disc.

DISC SIZE	DVD	CD	TYPE
8cm	1.4Gb	1.9Mb	SL/SS
	2.6Gb	X	DL/SS
	2.9Gb	X	SL/DS
	5.3Gb	X	DL/DS
12cm	4.7Gb	680Mb	SL/SS
	8.5Gb	X	DL/SS
	9.4Gb	X	SL/DS
	17Gb	X	DL/DS

Figure 13 – DVD Multi-Layered Capacities

User Self Diagnostics (VN02)

Description

The VN02 products have this feature. The End User/Dealer Self Diagnostics work without the need for other equipment. A number of hardware tests are automatically executed to check for faults in the recorder. The final test, number one, routes video to the Composite Out jack. The signal is a Pal Color bar signal. Most televisions will show the bars in B+W. This is dependent on the pull in range of the monitor, as the frequencies are shifted as compared to NTSC. The diagnosis ends with a “FAIL” or “PASS” message.

If the message “FAIL” appears on the display, an Error Code is displayed. If the message “PASS” appears, the tests have been executed successfully. There can still be a failure in the recorder.

The tests do not cover the complete unit. The following list describes the tests being performed while the test number is being displayed on the Front Panel.

To place the unit in the Self Test Mode, hold the Play pushbutton on the Front Panel while suppling AC power to the unit. The word BUSY appears on the display followed by test number. The display counts down numerically to test if it is performing.

The following is a list of the tests.

“Test Number” is displayed on the Front Panel
“Name” of the test
Description of the test

22
SdramWrR
Checks all memory locations of the 4Mbyte SDRAM

21
HostdDramWrR
Checks all the DRAM connected to the microcomputer on the Digital Board

20
HostdI2cNvram
Checks the data line (SDA) and the clock line (SCL) of the I2C bus between the host decoder and NVRAM

19
SAA7118I2c
Checks the interface between the Host I2C controller and the SAA7118 Video Input Processor

18
VideoEncI2c
Checks the interface between the host I2C controller and Empress

17
AudioEncI2c
Checks the I2C connection between the host decoder and Empress

16
AudioEncAccess
Tests the HIO8 interface lines between the host decoder and the audio encoder

15
AudioEncSramAccess
Checks the access of the SRAM by the audio encoder (address and data lines).

14
AudioEncSramWrR
Tests the SRAM connected to the audio encoder

13
AudioEncInterrupt
Tests the interrupt line between the host decoder and the audio encoder

12
VsmAccess
Checks whether the VSM interrupt controllers and DRAM are accessible

11
VsmInterrupt
Checks both interrupt lines between the VSM and the host decoder

10
VsmSdramWrR
Tests the entire SDRAM of the VSM

9
Clock11.289MHz
Switches the A_CLK of the micro clock to 11.2896 MHz

8
Clock12.288MHz
Switches the A_CLK of the micro clock to 12.288 MHz

7
BeS2Bengine
Checks the S2B interface with the Basic Engine by sending an echo command

6
DisplayEcho
Checks the interface between the host processor and the slave processor on the display board

5
AnalogEcho
Checks the interface between the host processor and the microprocessor on the Analog Board

4
AnalogNvram
Checks the NVRAM on the Analog Board

3
Tuner
Checks whether the Tuner on the Analog Board is accessible

2
LoopAudioUserDealer
Tests the components in the audio signal path: The host decoder on the Analog Board, the audio encoder, the VSM. The Audio is internally looped back thru the Digital Board

1
LoopVideoUserDealer
Tests the components on the Video signal system path: - The VIP- The Video encoder- The VSM- The host decoder. The Analog Board On Video signal is internally routed back to the Digital Board.

User Self Diagnostics (VN04)

The User Self diagnostics in the VN04 product are very different than the VN02 product. It has a different Digital Board.

Press **Play** and apply AC power. The display will flash quickly through a more technical display of the Nucleus (test) it is performing. If an error is found, the Nucleus Code and an Error Code will be displayed. Use the Service Manual to look up the code.

Manual Diagnostics VN02

Description

The VN02 products have this feature. The Manual Diagnostics provide the opportunity to perform tests and exercise the unit in a way that helps determine which of the DVD recorder's circuit boards are faulty. If no Errors are found, it performs an endurance loop test.

To successfully perform the tests, the DVD recorder must be connected to a monitor via the video out. The Servicer must respond to what is seen and heard on the monitor. (i.e. to approve a test picture or a test sound). Some tests require that a DVD+RW disc be inserted.

Structure of the Player Script
The player script (Manual Diagnostics) tests the circuit boards in the DVD recorder: the Display PCB, the Digital PCB, the Analog In/Out PCB and the Basic Engine.

The Player tests are done in two phases, interactive tests and a burn in test. The interactive tests depend strongly on user interaction and input to determine the results and to progress through the full test. The Burn-in Loop test will perform the same set of tests as the dealer test, but it will loop through the list indefinitely. Is is especially useful if you reset the Error Log. You can do this using ComPair. You can then read the error codes using ComPair.

Step by Step Description

1
Press **OPEN/CLOSE** and **PLAY** buttons at the same time and provide AC to the recorder to start the player script. Press **Play** to perform the test described on the display. Press **Stop** to skip the test and go to the next test. Press **Record** to indicate to the Microcomputer the desired result malfunctioned.

2
The display shows **FP SEGM**. Press PLAY to start the test. First the starburst pattern is lit. Press **Play** each time to advance. Then the horizontal segments are lit, followed by the vertical segments and the last test lights all the segments. After each of the four tests, the user has to confirm that the correct pattern was lit. Pressing **PLAY** confirms the correct pattern was lit. Pressing **RECORD** indicates that the correct pattern was not successfully lit. Press **STOP** to skip this or any test.

3
The display shows **FPLABELS**. Press **PLAY** to advance. All labels should be lit.

4
The display shows **FPLIGHT ALL.** Press **PLAY** to advance. Everything should be lit.

5
The display shows **FP LED**. Press **PLAY** to advance. The red Record light comes on. Press **PLAY** to confirm it lit. Press **STOP** to skip this test.

6
The display shows **FP KEYBRD**. All keys have to be pressed to get a positive result! This includes the Power button. Press **PLAY** for more than two seconds to confirm that all the keys were pressed and that it was shown on the display. Press **STOP** for more than one second to skip this test.

7
The display shows **FP REMCTL.** Press **PLAY** to confirm that a key on the remote control was pressed and shown on the local display. Only one key has to be pressed to get a successful result.

8
The display shows **FPDIMMER**. Press PLAY to activate the dimming feature. Press Play to confirm that the text on the local display was dimmed.

9
The display shows **ROUTE VID**. Press **PLAY** to advance.

10
The display shows **ROUTE AUD**. Press **PLAY** to advance.

11
The display shows **COLORBAR ON**.Press **PLAY** to advance. An NTSC Colorbar Pattern should appear at the output. Press **PLAY** to advance.

12
The display shows **PINKNOISE ON**. The monitor should produce Pink noise.

13
The display shows **PINKNOISE OFF**. Press **PLAY** to advance.

14
The display shows **BE RESET**. Press **PLAY** to Reset the Basic Engine (Mechanism/Servo PCB).

15
The display shows **BE TRAY OPEN**. Press **PLAY** to open the tray. Place a RW disc in the tray.

16
The display shows **BE TRAY CLOS**. Press **PLAY** to close the tray.

17
The display shows **BE WRITE READ**. This requires a RW disc to be in the machine. The BE resets and a small write is preformed, and then a read. This will take 20 seconds or so.

18
The display shows **BE TRAY OPEN**. This opens the tray.

19
The display shows **BE TRAY CLOS**. This closes the tray.

20
The display shows **ERRORLOG READ**. If there was an error, a code will be displayed. If you press **PLAY**, the diagnostic script will start an endless loop. If the unit fails a test, the local display will display FAIL and the error code.

In case of a failure, the display shows “ **FAIL XXXXXX** “The description of the shown error code should be found in the list in the Service Manual. Once an error occurs, press the **STOP** key to jump over the failure and to continue the diagnostics.

There is a Error Code Table in Force Manual 2064.

VN04 product does not have Manual Diagnostics.

If you try to place the unit in diagnostic mode in the same manner as the VN02 product, there is no display and the unit is locked.

Overall Block

Key Components

The unit is made up of: the Power Supply/Analog Board, the Front Panel, the Basic Engine, the Digital Board, and the Digital Video Input/Output Board. Refer to **Figure 14.** The DVIO board's circuitry is contained on the Digital Board of the VN04 product.

Block Diagram Descriptions

Power Supply
The Power Supply is a SMPS using Hot Ground on the primary side of the transformer. There is no MAINS power switch. It is operating when AC is applied. It supplies power to: the Analog Board, the Digital Board, the Basic Engine, and the Front Panel..

Front Panel Display
This module contains a microcomputer that doubles as a fluorescent display driver. It receives the IR inputs and the keyboard inputs. It communicates the user input from the Keyboard and IR Receiver via the I^2C Bus to the Microcomputer on the Analog Board.

Basic Engine (BE)
This consists of the Mechanism and Servo control PCB. The Mechanism is essentially the same as a DVD with the exception of the Optical Pickup Unit, OPU. The OPU has a dual direction signal and light path, one for the write signal and one for the play signal. The OPU has three ICs mounted on it for processing laser signals. These include: the Laser Drive IC or LADIC, the Dvd Recordable Optical Preprocessor IC or DROPPI, and the Non-Volatile RAM or NVRAM to store its electro-mechanical settings.

The Servo controls the Mechanism. It handles the HF signal to and from the OPU. It uses a Microcomputer to control all aspects of the Servo operation. This includes: tray operation, spindle speed, focus, HF preprocessing, and radial positioning of the OPU.

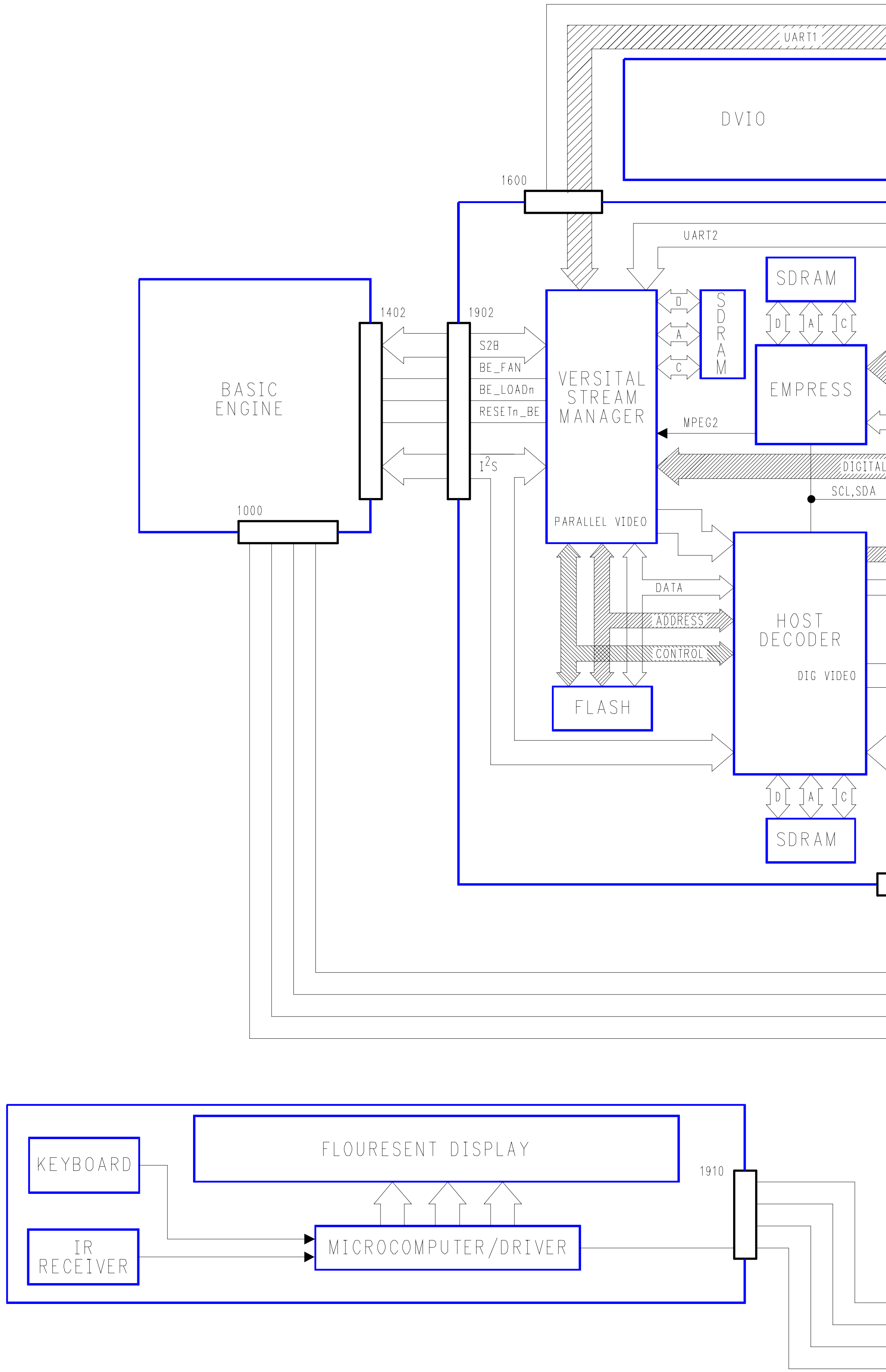
Digital PCB

This module performs many functions. It interfaces between the Basic Engine and the rest of the unit. There are two Digital Boards in the DVDR75. The Product Number is different signifying which Digital Board is in the unit. The one described here is the VN02 product. The functionality and connections are the same. The VN04 product contains the DVIO circuitry, and a different chipset. A separate block diagram follows the Digital Board's Circuit Description.

During record, it encodes analog video and digital audio into a recordable digital data stream. The Analog to Digital Converter for video is part of a Video Input Processor, VIP, that supplies the MPEG2 Encoder. The VIP sends parallel digital video to the EMPRESS and the VSM. The Empress is the MPEG2 Encoder. It receives video from the VIP and audio from the Analog Board. The Audio is A/D converted on the Analog Board. The EMPRESS is a microcomputer. It has its own SDRAM. It supplies MPEG2 data to the VSM, Versatile Stream Manager. Using sync from the Digital Video coming from the VIP, the VSM converts the signal into an I squared S serial signal. The serial data is sent to the BE to be recorded on the disc.

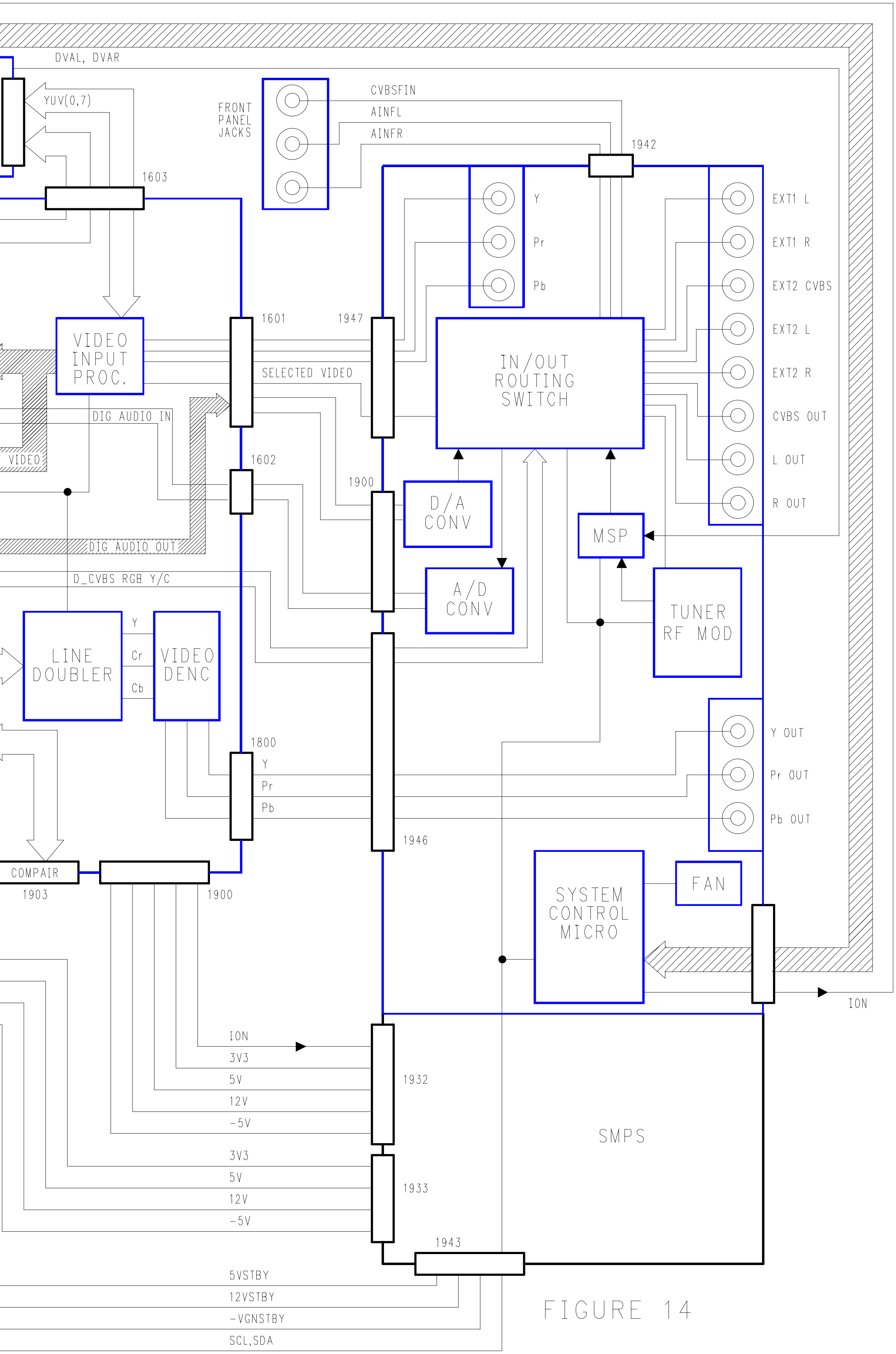
During playback, the MPEG2 Decoder receives its I squared S input directly from the BE. It decodes the data stream into analog Video and digital Audio. Both are sent to the Analog Board. Digital Video is provided to the Line Doubler. The Line Doubler receives 11 bit digital YUV. The Line Doubler produces progressive scan digital Y/U/V that goes to the Digital to Analog Encoder. Y, Pr, and Pb are sent to the Analog Board.

The Host Decoder is the Master of the I squared C bus that provides communication between the Microcomputers: Empress, VIP and the Line Doubler. The VSM Communicates to the System Control Microcomputer Via UART1. UART2 provides communication between the Digital Board and the DVIO Board. EMI uses Flash memory to provide the Boot up sequence and the operational firmware. Updates can be loaded to



UART1
DVIO
1600
UART2
SDRAM
BASIC ENGINE
1402
1902
S2B
BE_FAN
BE_LOADn
RESETn_BE
I2S
VERSITAL STREAM MANAGER
PARALLEL VIDEO
D
A
C
SDRAM
EMPRESS
MPEG2
DIGITAL
SCL,SDA
1000
DATA
ADDRESS
CONTROL
FLASH
HOST DECODER
DIG VIDEO
SDRAM
KEYBOARD
FLOURESENT DISPLAY
1910
IR RECEIVER
MICROCOMPUTER/DRIVER

Figure 14 – C



Overall Block

enhance operation of the unit. At present, the update disc is version 6.1.

Analog PCB
This module contains: the Power Supply, the System Control Microcomputer, all the A/V inputs and outputs including a Tuner/RF Modulator. Source selection and output type are controlled by the microcomputer. The microcomputer controls many functions throughout the unit including: Power up, user input, input/output selection, the Tuner, the D/A, and A/D functions of the Audio. It also controls the Fans.

Input selection is an important function performed by the analog board. The user selects between: External 1 and 2, DVIO, Tuner Video, and Front Panel jacks.

Audio processing is performed on the Analog Board. The Audio signal coming from the Tuner has a separate demodulator. The Multi System Processor, MSP, demodulates the audio and sends the signal to the Routing Switch. The MSP selects between Tuner Audio and the DVIO Audio signals. The selected audio is sent to the A to D Converter. Digital Audio is supplied to the Digital Board for recording.

DVIO PCB
The Digital Video Input Module provides IEEE 1394 translation to the DVD recorder. It separates the Digital Video and Audio. The Digital Audio is decoded and sent as Analog Audio to the Analog Board. Digital Video (DV) is supplied to the Video Input Processor on the Digital Board. The DVIO board communicates with the Digital board via UART2.

Power Supply

This unit uses a Switch Mode Power Supply, SMPS. It operates whenever ac is applied. A MOSFET transistor turns On and Off in an oscillator fashion, driving a transformer. The primary half of the supply uses a Hot Ground. The primary side of the circuit provides drive and coarse control of the power supply. The secondary side of the circuit rectifies and filters the output of the transformer to produce many output voltages. It uses a cold ground, signal ground system. The output is monitored for precise regulation. The 5Vdc is supplied to the anode of the Optic Coupler's diode and fed to the Shunt Regulator. The regulation path includes an Optic Coupler to accommodate the different grounding systems.

Circuit Description

AC Input Circuit
The AC input is rectified by diodes 6301, 6302, 6305, 6306, and filtered by C2309. Refer to **Figure 15**. The voltage on C2309 is approximately 155V. It can vary from 150V to 160V, depending on the AC input voltage.

Start Circuit
The start up of this power supply is mostly contained in IC7313. The Drain supply voltage goes to Pin 8 of the IC. The running supply for the IC is Pin 1 of the IC. The Supply Control provides a measured supply to the VCO and the Driver for start up. The power supplied is not enough to keep the unit operating. If the supply does not operate and supply Pin 1 with operating power, the unit stalls.

When the power plug is connected to AC, the MOSFET 7307 will start conducting when the gate voltage reaches the threshold value. A current starts to flow in the primary winding of 5300, Pins 7 and 5. While the MOSFET is conducting, energy is building up in the transformer. The current flow through the MOSFET is sensed by R3352, and 3321. When the current level rises high enough to provide a voltage drop on these components, 7307 is turned Off by the driver circuit. Diode 6311 protects the control circuit in

case of failure of the MOSFET by providing an upper-limit to the voltage that can remain on the source of the MOSFET.

Coarse Regulation
The positive portion of the signal on Pins 2 and 3 will be rectified via D6316, charging C2325. In time, the voltage on C2340 will reach 9 to 13Vdc. This value depends on the value of the Mains voltage and the load. This is also used as a regulation supply for the optic coupler IC7314.

The control circuit consists of a VCO, the Driver, an Op Amp and Gate that are fed by the sensing resistors, 3352 and 3321, and C2340. This circuit controls the conduction time and the switching frequency of the MOSFET. It switches Off the MOSFET as soon as the voltage on the source of 7307 reaches a certain value.

Demagnetization or complete magnetic field collapse is desired before the next drive signal is applied to the MOSFET. This improves efficiency by reducing the power necessary to build a magnetic field in the transformer. Pin 4 is the Demag input. When Pin 4 is near 0Vdc, the gate is enabled, allowing the next oscillation to occur.

Secondary Rectifier/Smoothing Circuit
There are six Rectifier/Smoothing circuits on the secondary side. Each supply voltage depends on the number of windings in the transformer. From these circuits, several voltages are derived.

Precise Regulation
The 5VREG is monitored for regulation. The regulation circuit consists of an Optic-Coupler, 7314, a shunt regulator, 7315, and a voltage divider network. The Optic-Coupler isolates the Hot Ground on Pin 2 of 7313 from the Cold Ground voltage on 7315. 7315, a Shunt Regulator, has two component characteristics. It is a very stable and accurate reference diode and a high gain amplifier.

7315 will conduct from cathode to anode when the 5VREG is rises higher than the 5Vdc. The 5VREG is divided down to a 2.5V reference voltage. If the 5VREG and subsequently the reference voltage is lower, the cathode current is almost zero. The cathode current flows through the LED of the Optic-Coupler, controlling the current through the transistor portion of the Optic-Coupler. The collector current of 7314 will adjust the feedback level of the error voltage at Pin 3 of 7313.

There are standby and switched supplies. The 5VSTBY, 12VSTBY, 5NSTBY, 33VSTBY and the VGNSTBY supplies are always present when AC is supplied. The VGNSTBY supply ia a -33Vdc dedicated to the Front Panel Fluorescent Tube as a grid supply. The 5SW, 8SW, 12V, 5V, and 3V3 supplies are switched.

The STBY control voltage switches On the 5SW and the 8SW. As part of the first layer of Power Up, the System Control Microcomputer pulls the STBY line Low. This removes bias to 7308 and 7321. This allows the standby supplies to bias 7319 and 7320 On. These supplies go to the RF Unit, the Sound IF and the Input Matrix.

The ION control voltage turns the unit On and Off. When the user turns the power On, the ION control voltage goes Low, turning 7306 Off. The 33VSTBY supply is allowed to turn On 7318. The switched 12V becomes available. The Switched 12V switches On the 3V3 and the switched 5V supplies. The 3V3 and 5V supplies are regulated by shunt regulators, controlling MOSFETs.

Overcurrent Protection Circuit
When the output is shorted, the current through the FET will produce a large voltage drop across the source resistors of the FET. When Pin 5 is elevated, the Op amp's output is low, disabling the output of the Driver. This switches Off the drain current of the MOSFET, 7307. The start circuit will try to start up the power supply again. If the short still exists, the complete start and stop sequence will repeat. The power supply is in a hiccup mode and is ticking.

Overvoltage Protection Circuit
If the regulation circuit does not function due to an error in the control loop, the regulated output voltage will increase. This overvoltage is sensed

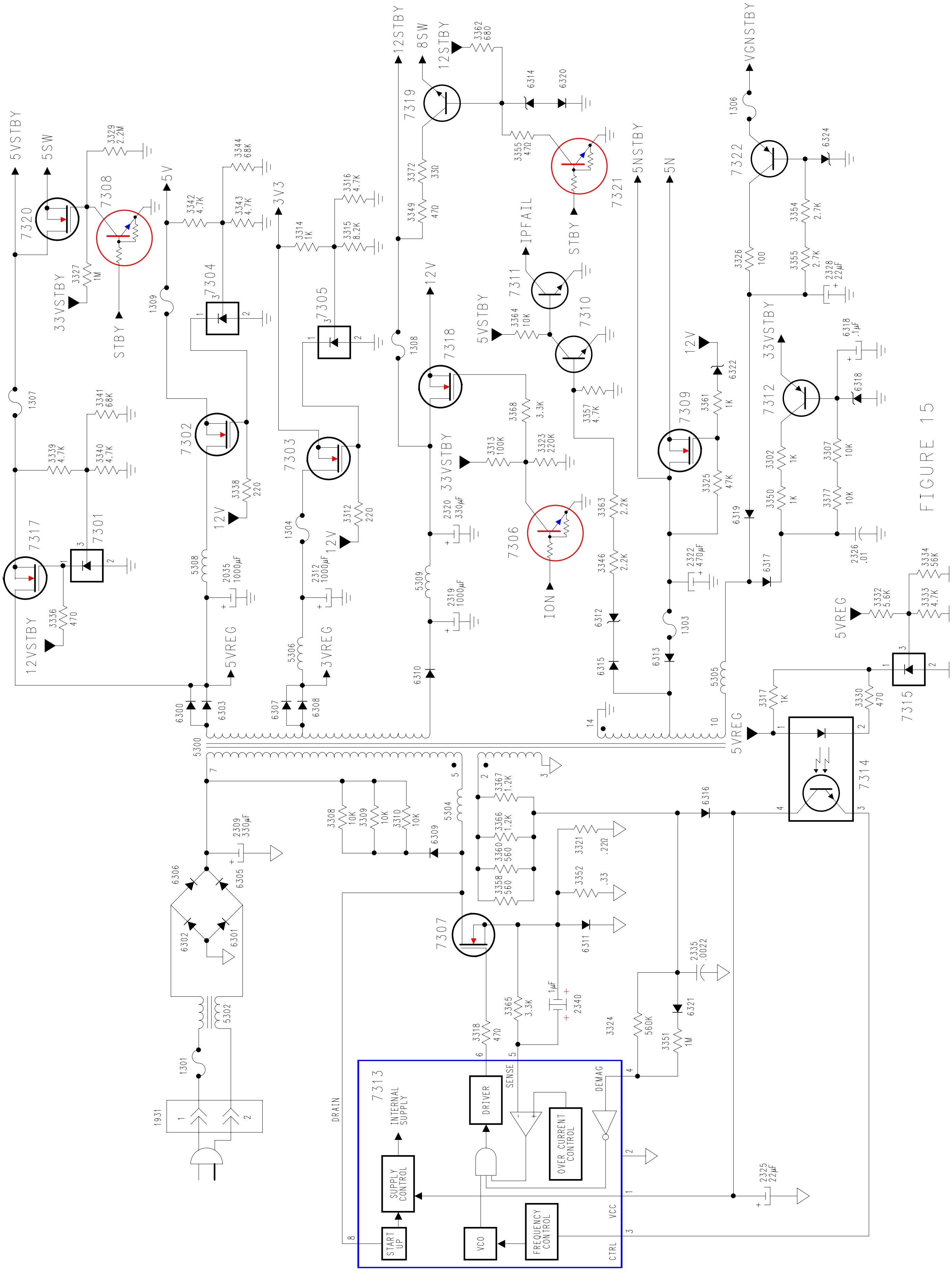


Figure 15 - Power Supply Circuit

on the hot ground side of the transformer at Pins 2 and 3. When an overvoltage is detected, the Demag circuit will activate the inverter. The power supply will be shutdown until the voltage returns to zero. it will then try to restart.

The IPFAIL signal is used as a Power Fail measurement signal. During normal operation, 7310 is biased On by 6315 and 6312. When power is interrupted that Bias is removed prior to the Filter capacitors draining off their charge. 7310 turns Off, allowing the 5VSTBY to turn On 7311. The IPFAIL goes low. This signal goes to the System Control Microcomputer and Mute circuits.

Microcomputer

The Microcomputer, IC7804, is a 16-bit processor with internal ROM and 4kB RAM. It uses External RAM, IC 7803, and Flash, IC 7805. It is mounted on a Sub Board soldered into the Analog Board. Refer to **Figure 16**. The System Clock operates at 24MHz. It uses an I^2C interface to communicate with the other Microcomputers in the unit. The clock rate is approximately 95kHz. The Reset Pin is high during normal operation. The microcomputer uses non-volatile EEPROM, 7805. The EEPROM stores data specific to the device, such as the AFC-reference value, clock-correction-factor, etc.

Power up

7804 controls power up of the unit. There are three layers to the power up sequence. The first layer involves the Analog Board and the Front Panel. The second layer involves the Digital Board and the BE. The third involves the Front Panel and the Analog Board.

The first layer controls the first set of switched supplies. After the System Control Microcomputer receives its reset, the STBY control voltage goes Low to turn On the first set of switched supplies, the 5SW and the 8SW. It communicates on the I^2C bus initializing the RF Unit, the Sound IF, and the Input Matrix ICs. If they respond properly, it then communicates on the I^2C to the Front Panel Microcomputer. If the Front Panel Microcomputer responds properly, the ION control voltage goes Low.

The second layer occurs when the ION switching voltage goes Low. It comes from the System Control Microcomputer. The ION control voltage passes through the Digital Board to the Power Supply and turns On a second set of switched voltages. These include the 3.3Vdc supply. The 3.3Vdc supply is the main B+ to many of the microcomputers throughout the unit. The System Control Microcomputer then sends out the IReset signal to 7902 on the Digital Board. This IC produces a delayed Resetn signal line for 7200. 7200 activates its I^2C and provides several reset and initialization signals for the Digital Board, DVIO, and the BE. They all go through a self test. If the self test succeeds, the VSM communicates through UART1 that the system is operating, and the unit can enable the Front Panel to accept a response. The Front Panel Microcomputer then places four dashes on the Front Panel Display. ION goes High placing the unit in Standby, waiting for keyboard input. This normally takes 6-8 seconds. The System Control Microcomputer allows 10 seconds for the UART1 response. If it does not come, the unit goes into sleep mode, and will not accept keyboard input.

When the Front Panel Microcomputer receives a keyboard response, it communicates that action to the System Control Microcomputer to switch back On the second layer of switched voltages.

The System Control Microcomputer controls the operation of the entire unit. It uses UART1 for communication with the Microcomputers on the Digital Board. It uses the I squared C Bus ,I^2C to communicate with devices on the Analog Board. It receives composite sync from the Selected video source. This is to determine that a good signal source has been selected before the unit is allowed to record.

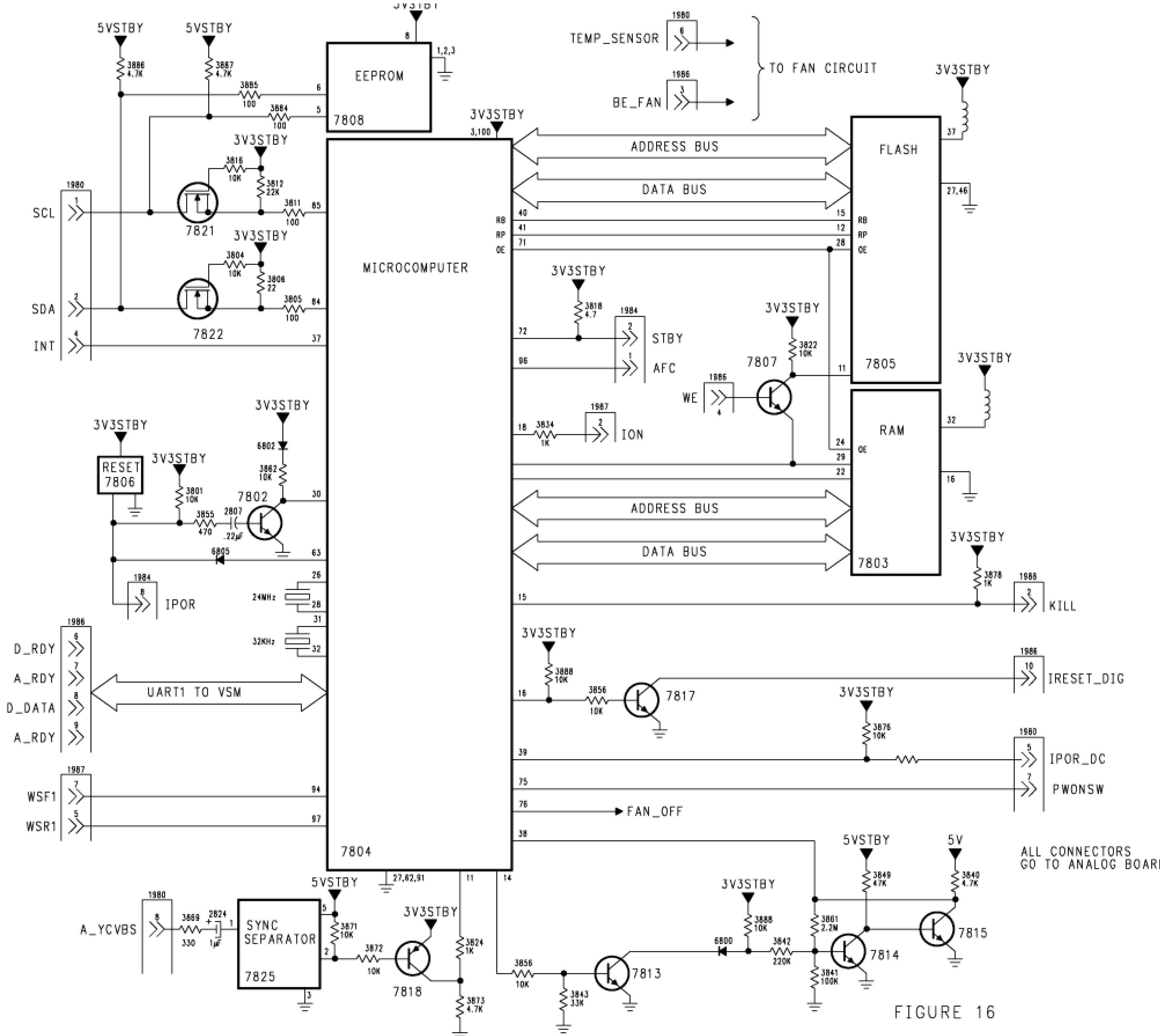


Figure 16 - System Control Microcomputer

Front Panel

The main elements of the Front Panel are the microcomputer, 7103, the Display Tube, and the keyboard. Refer to **Figure 17**. 7103 is an 8-bit microcomputer fitted with 96kB ROM and 3kB RAM and is responsible for the following functions:

Fluorescent Display driver

Monitoring the keyboard matrix

Communicating with the System Control Microcomputer

Decoding the remote control commands from the infrared receiver, 7107.

Activation of the display

The Fluorescent Tube operates using a grid and segment scanning matrix. AC is supplied by a switching regulator consisting of 7106, 7108, and 7109. A squarewave is produced by the Microcomputer on Pin 19. The Signal is amplified by 7109 and supplied to the Push/Pull output Amp.The signal passes through 5104 going to the tube. With AC supplied, the microcomputer scans the elements in the tube to determine what segments light up. The system clock is generated with the 8MHz crystal, 1100.

Keyboard Matrix

There are 6 keys on the display board and 1 on the Standby board. A resistor network is used to generate a specific voltage value, depending on the key pressed, via the resistors 3300, 3103, 3104, 3106, 3108, 3110, and, 3130. This RTL data (voltage Level) is sent to 7103 on Pins 36 and 37. Pressing keys simultaneously may lead to undesired functions.

Communication with the System Control Microcomputer occurs on a I Squared C bus, SDA and SCL. The Front Panel receives standby supplies, so it is always live when AC is suppled to the set. The System Control Microcomputer Hosts the I squared C Bus. The System Control resets and initiates the I squared C bus. The Front Panel Microcomputer resets simultaneously and communicates to the System Control Microcomputer that It is operating. The push buttons and IR receiver are then monitored.

IR Receiver

The IR receiver, 7107, contains a bandpass amplifier as well as a photo-diode. The photodiode receives approximately 940nm infrared pulses. The pulses are amplified and demodulated. On the output of the IR receiver, 7107, is a pulse sequence at TTL levels. The IR signal appears on Pin 20 of 7103.

The Front Panel contains a Thermal Sensor. It is a temperature coefficient resistor. As the temperature rises, so does the resistance. This voltage is sent to the Fan Control Circuit.

The Record LEDs are controlled by the Front Panel Microcomputer. 7105 and 7112 are the LED drivers. Pin 3 of the microcomputer goes low to turn on the lights. That turns On 7112 which in turn turns On 7105. 7105 pulls current through the diodes illuminating them.

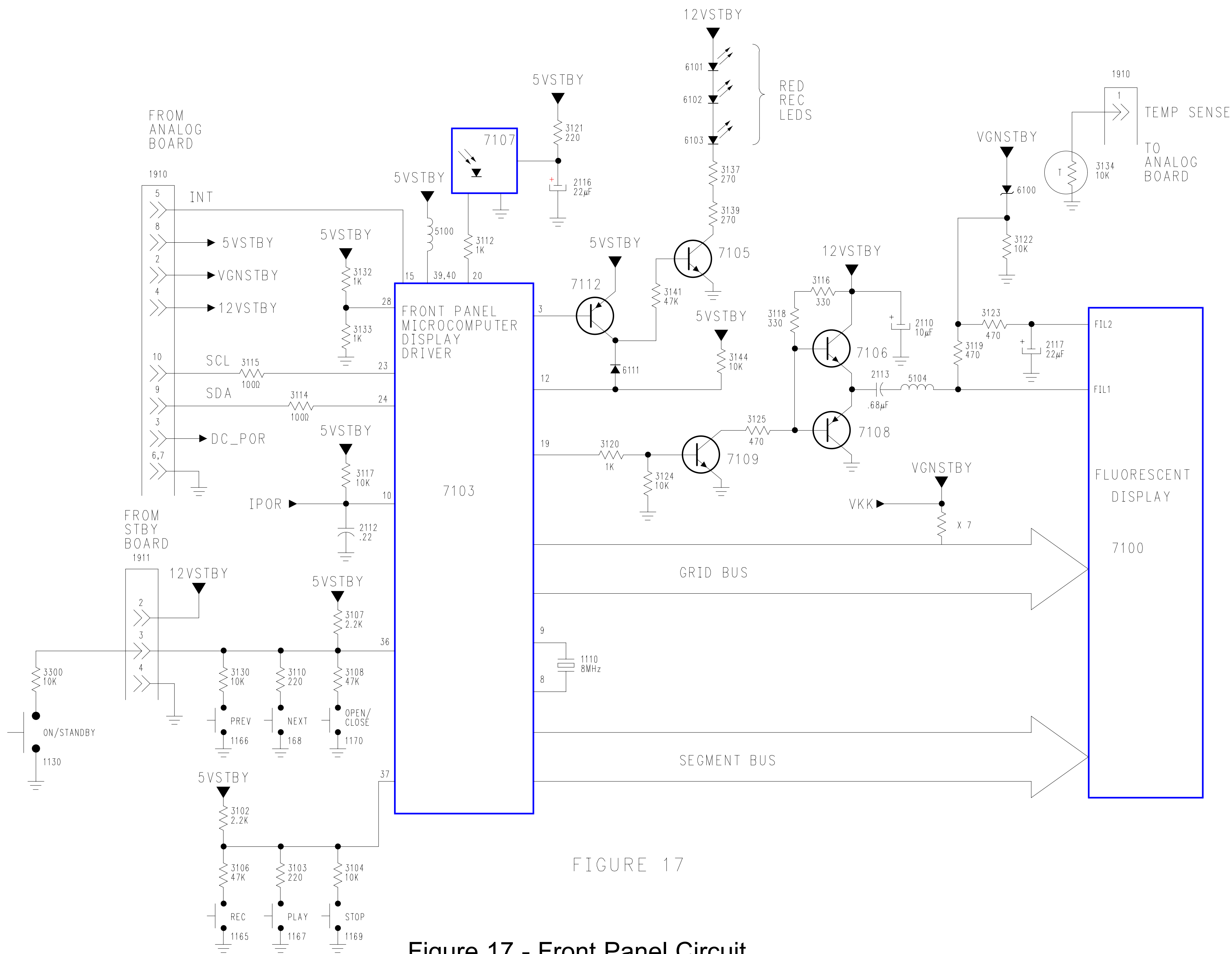


Figure 17 - Front Panel Circuit

Analog Processor Board

The Analog Board controls all analog input/output selection, and routing. It houses the System Control Microcomputer. The System Control Microcomputer controls the routing and other functions on the board. One of its other main functions is to control power and initialization of the unit. It implements Keyboard instructions. The board has the Optical Audio Out and the Coax Digital Audio Output circuits. It controls the Tuner. The Audio D/A and A/D conversion is performed on this Board. It contains the Fan Control circuit and houses the first Reset circuit for the System Control Microcomputer.

There are three circuits that can Mute the audio. The Digital Board produces the D_KILL signal. There is a power fail circuit, which is necessary to mute AUDIO when power is lost, IPFAIL. The System Control Microcomputer produces the Kill signal.

Tuner/RF Unit

The Tuner is part of and RF Unit. It contains the Tuner, An RF Modulator and the Demodulator/IF. The Tuner is capable of receiving 125 channels, and is cable ready. Refer to **Figure 18**. The RF connections on the back are part of the Tuner, RF Modulator. The RF Unit receives two supply voltages, 33Vdc and SW5Vdc. The channel selection information is communicated via the I^2C lines. The output channel is selected by CSW_SSW control voltage. Video is output from Pin 24. 7700 buffers the signal before it goes to Input Matrix. The RF Unit does not perform audio demodulation. The audio signal leaves the RF Unit as Sound IF, from Pin 15 of the RF Unit. The Digital Board's output video, D_CVBS goes to the RF Unit for the RF Modulator to output the signal on channel 3 or 4. The audio signal returns to the RF Unit on Pin 2 to be used by the RF Modulator. The AFT signal comes from the Microcomputer.

Audio Demodulator

The Sound Processor, 7600, demodulates the Audio. MPS means Multi System Processor. The I^2C bus controls its operation. It uses two power supplies, the 5Vdc and the 8V Switched. IC 7600 has its own oscillator on Pins 5 and 6. Amplitude and bandwidth of the demodulated audio signals can be determined in 7600 using the I^2C bus. It sends analog audio back to the RF Unit from Pin 26. The audio coming from the Digital Board, ARDAC and ALDAC, go into the Sound IF. The I^2C bus controls what Audio is output, the Tuner Audio, or the Digital Board's output. The Audio signal output from the MSP is available at Pins 30, AFER, and 31, AFEL. 7600 controls the audio input selection via RAS1 and RAS2 switching voltages. They go to the Input Selection Switch, 7501.

7419 and 7420 perform level matching between the 5V serial clock and data lines of the Tuner and Demodulator to the 3.3V levels coming from the Microcomputer.

Input Matrix

The A/V I/O switching is controlled by a switching matrix, 7408. It is controlled via the I^2C Bus. The Matrix controls what source will be supplied to the Digital Board. There are several choices: Tuner Video, External 1(Y/Pr,Pb), External 2 Video, and Front Video. In addition there are 2 Y/C inputs. All switches have 6 dB amplification on the outputs. The Matrix is not responsible for handling the Y/Pr,Pb. It goes directly to the Digital Board when present.

The user selects what source is to sent to the Digital Board on Pin 9 of 1947. The I^2C Bus communicates this data to the Matrix IC. The selected source comes out Pin 21 of 7408. The Matrix communicates channel selection control for the RF Unit on Pin 44.

The unit can receive a 16 by 9 input using the Y/C inputs. The Microcomputer must detect this format and communicate it to the Digital Board.

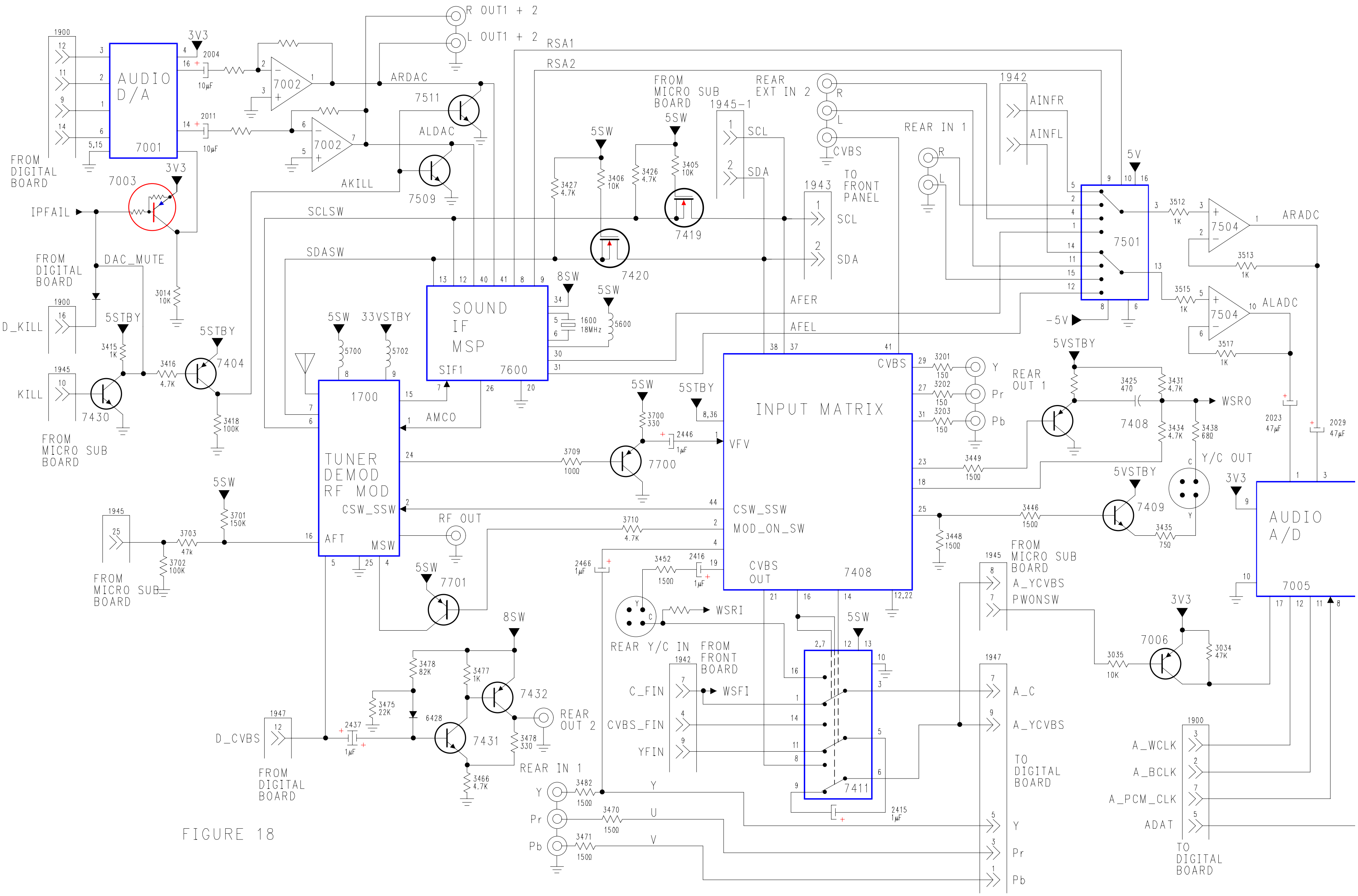


Figure 18 - Analog Board Block

This is done using the Chroma signal of the Y/C signal. The DC level of the Chroma is elevated 3.3V. The DC level is detected 2 places. Wide Screen Rear In (WSRI), and Wide Screen Front In (WSFI). The unit communicates the same thing to the monitor when outputting 16 by 9 using Wide Screen Rear Out, WSRO.

goes to the D to A Converter, 7001. The D/A converts the signals back to analog left and right audio, ARDAC and ALDAC. These signals go directly to the Audio Out jacks and the Sound IF IC 7600. The Sound IF selects what audio is supplied to the RF Unit.

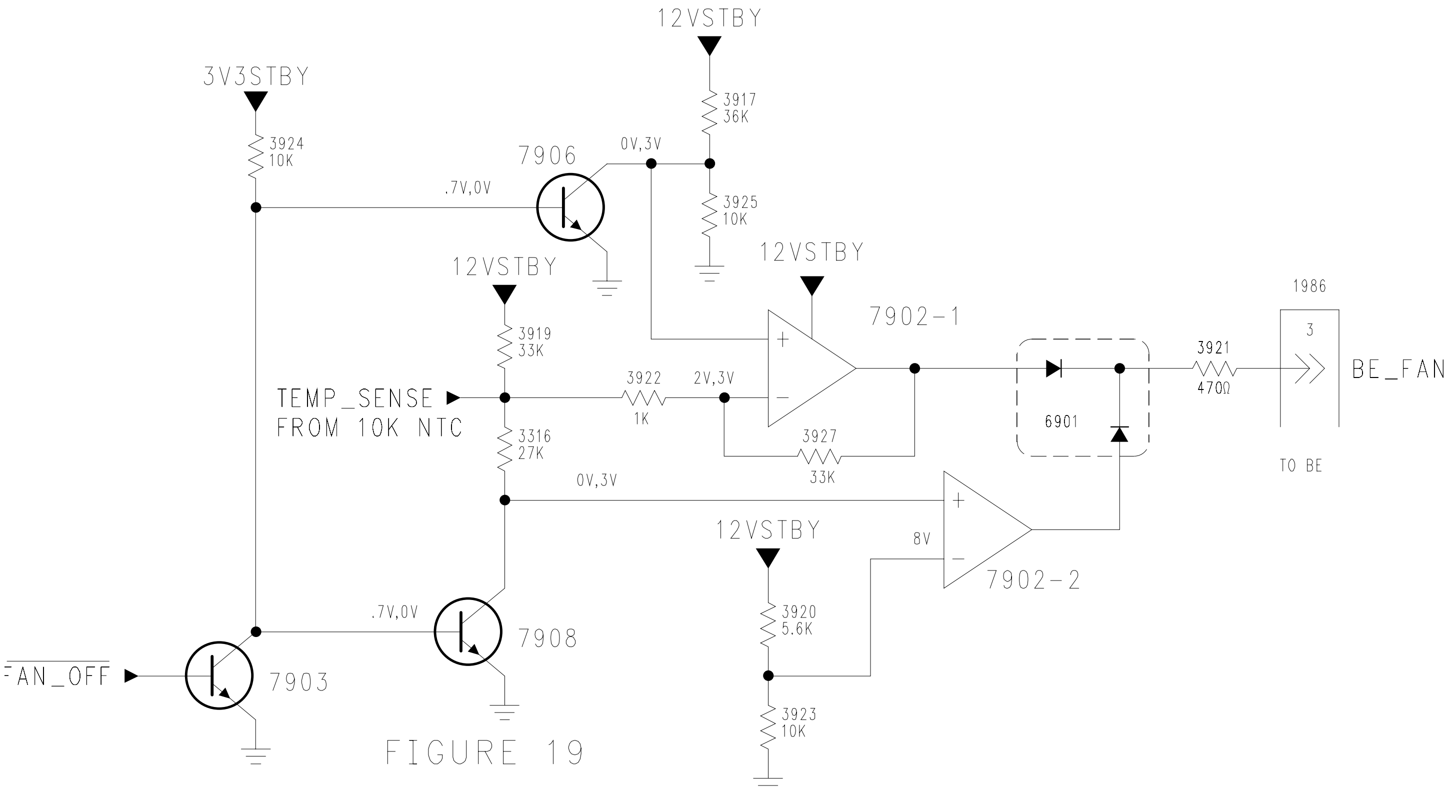


Figure 19 - Fan Drive Circuit

The Audio I/O switching is controlled by 7501 via the I^{2}C Bus using the Sound IF and 2 control lines, RAS1 and RAS2. Analog Audio coming from Rear External Inputs 1,2, Tuner Audio, and Front In are suppled to IC7501. 7501 selects the audio source to be sent to the A to D Converter. The A/D Converter uses the A_PCM_CLK to generate the Digital Audio signal sent to the DIgital Board a A_DAT on Pin 5 of 1900.

During playback and Powered On Standby, the Digital Board sends back to the Analog Board the same format of Audio as it received. This

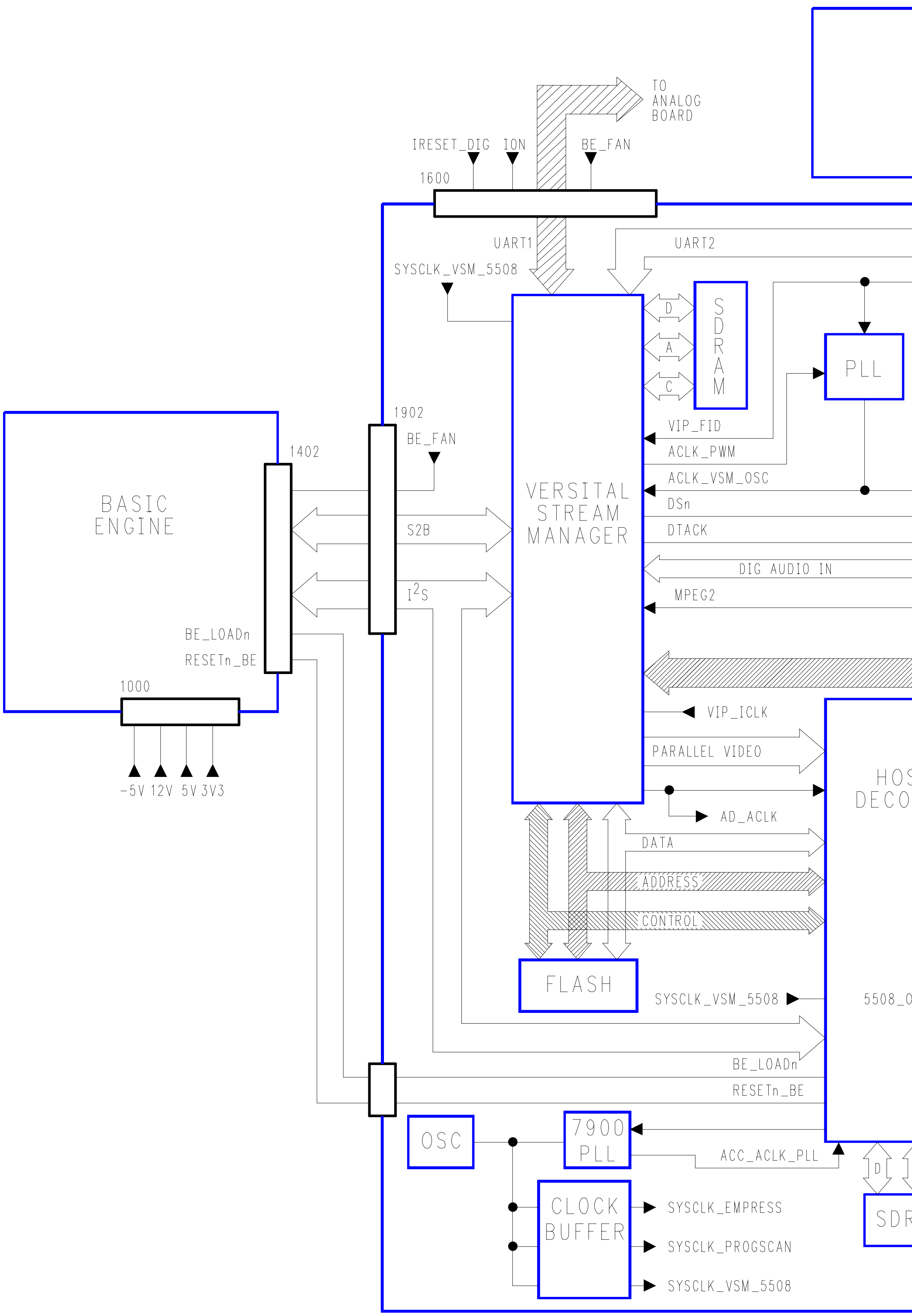
Fan Control

The Fan Control circuit is necessary to control the speed of the BE Fan according to the changes of operating temperature. The temperature is measured via a Negative Temperature Coefficient, NTC, thermistor on the Front Panel, 3134. The sensor's output voltage is labeled Temp_Sense.

The Fan Control circuit uses an Op Amp to amplify the BE_FAN signal. The Microcomputer controls the On/Off function of the fan via control line FAN_OFF. FAN _OFF goes Low to turn

Off the fan. When High, the Fan is turned On. 7903 is biased On, removing bias to 7906 and 7908. The divider resistors, 3917 and 3925 provide approximately 3Vdc to the non-inverting input to 7902-1. The inverting input receives a similar supply via 3919 and the 10K NTC resistor on the Front Panel. When the operating temperature is warm enough to decrease the resistence of the NTC, the inverting input will drop below the non-inverting input. The ouput of the Op Amp will go High. this high is sent to the BE to turn On the fan.

7902 is a saftey circuit. If the NTC were to open or be disconnected, the non-inverting input to 7902 would jump to approximately 12Vdc. this would turn on the fan any time the System Control's output FAN_OFF allowed the fan to operate.



TO
ANALOG
BOARD
IRESET_DIG
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BE_FAN
1600
UART1
UART2
SYSCLK_VSM_5508
D
A
C
SDRAM
PLL
VIP_FID
ACLK_PWM
ACLK_VSM_OSC
DSn
DTACK
DIG AUDIO IN
MPEG2
1902
BE_FAN
1402
BASIC
ENGINE
VERSITAL
STREAM
MANAGER
S2B
I2S
BE_LOADn
RESETn_BE
1000
-5V 12V 5V 3V3
VIP_ICLK
PARALLEL VIDEO
AD_ACLK
DATA
ADDRESS
CONTROL
FLASH
SYSCLK_VSM_5508
BE_LOADn
RESETn_BE
OSC
7900
PLL
ACC_ACLK_PLL
CLOCK
BUFFER
SYSCLK_EMPRESS
SYSCLK_PROGSCAN
SYSCLK_VSM_5508

FIGU

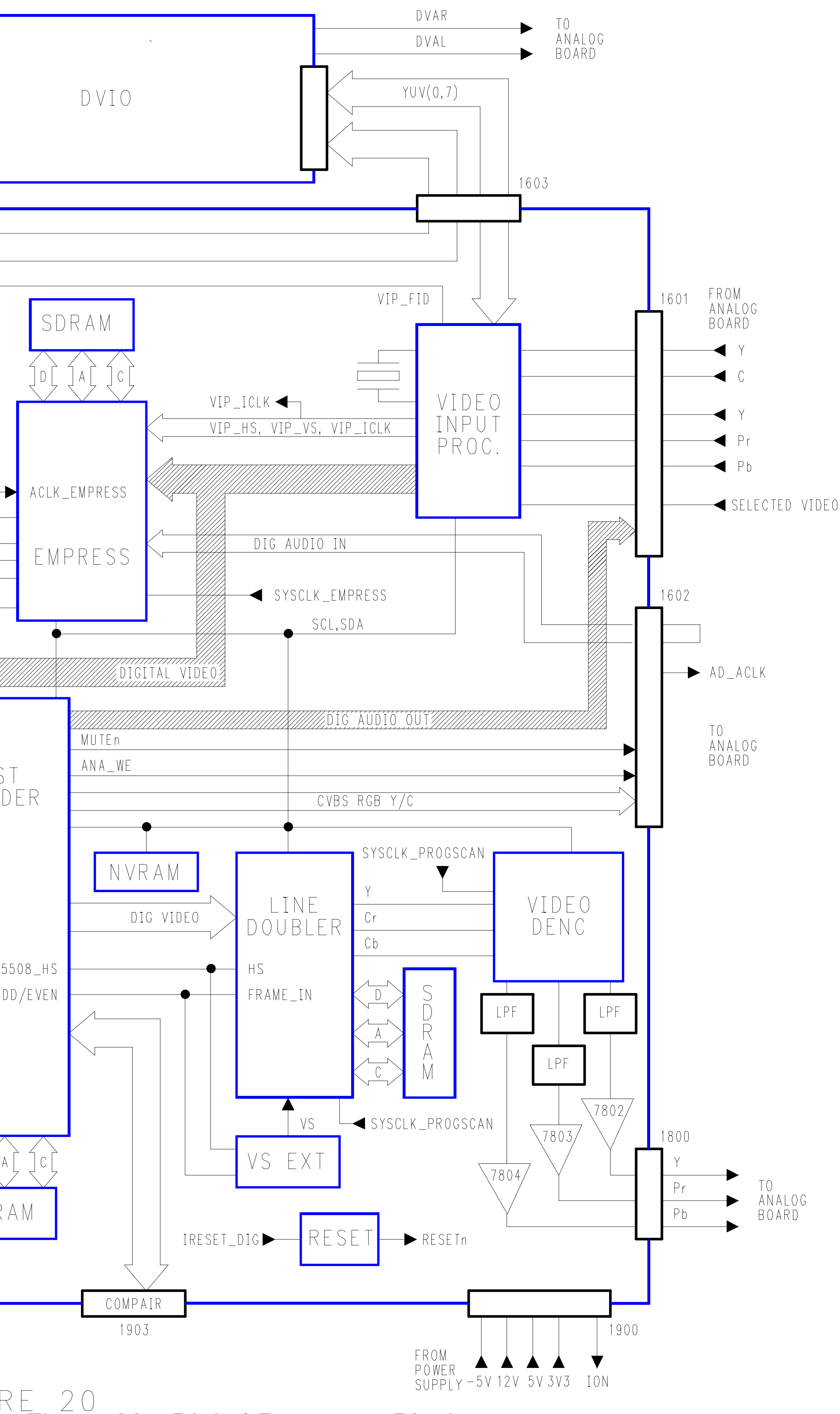


Figure 20 - Digital Processor Block

Digital Signal Processor VN02

The Digital Signal Processor has many responsibilities. Refer to **Figure 20**. It is responsible for encoding Digital Video and Audio into MPEG2 and AC3 respectively. It supplies MPEG2 and AC3 via an I squared S serial protocol to the Basic Engine (BE) for recording. It also receives the MPEG2 Video via I^2S from the BE, decodes the signal, and supplies Digital Video to the Progressive Scan circuit. It supplies Analog Video to the Analog Board, and Digital Audio (I^2S) to the Analog Board. The entire operation starts with the B+ supplies and the System Clocks.

Most of the data going to the BE passes through the Versatile Stream Manager, VSM. The VSM is a microcomputer, using SDRAM to preform its functions. The Empress supplies MPEG2 Video to the VSM. The VSM combines the Audio and Video into one data stream. The VSM is a hub for data streams. The VSM also sends the Digital Video/Audio Data to be recorded back through the playback signal path. This output from the VSM is called the Parallel Digital Video path. Most of the data going to and from the Digital Board and the BE goes through the VSM. The exceptions are the Digital Video Playback Stream, and some control signals. The S2B signal communicates most of the control signals to the BE. The Reset and Download control signals come from the Decoder. The I squared S playback stream goes directly to the MEG2 Host Decoder, IC7200.

The MPEG2 Decoder IC7200 contains a microcomputer. It uses SDRAM to perform its functions. It is the Host to the I squared C Bus, I^2C. Using the I^2C Bus, the Host Decoder is the System Control of the Digital Board. It controls the following IC's: IC7100, IC7403, IC7500, IC7700, and IC7801. The I^2C Bus is the major communication avenue for the Digital Board. The Host Decoder communicates to the Analog Board's Microcomputer Via the VSM using the EMI.

The Decoder's second responsibility is signal processing. The Decoder receives the Parallel video and the BE's I^2S signal. One or the other will be present at all times, depending on whether the unit is in powered up Standby, Play or Record. The Decoder separates the Video and Audio, then Demodulates the MPEG 2 video into several outputs. It produces Composite Video, Y/C, and RGB to be sent to the Analog Board. It produces an 8-bit digital Y/UV for the Progressive Scan circuit. It produces two types of Audio, I^2S and SPDIF. They both go to the Analog Board.

The Progressive Scan, Pscan, circuit sends Y/Pr/Pb analog, 480P, Video to the Analog Board to be provided to the output jacks. The Pscan, circuit contains a Line Doubler and a Digital Encoder. The Line Doubler receives the 8-bit Y/UV from the Decoder. It doubles the vertical scan lines and produces separate Y, U, and V. 10-bit Y, U, and V are translated into analog Y, Pr, and Pb by the Digital Encoder. The signals are passed through Low Pass Filters to remove any switching noise left in the signals. The signals are amplified before they are sent to the Analog Board.

EMI Bus

The VSM and the MPEG2 Decoder share a Data Bus called the External Memory Interface, EMI. The EMI contains 4 Megabytes of Flash EEPROM. The EEPROM contains the firmware for the Digital Board. The firmware contains the boot ROM and software for the two microcomputers.

The Digital Video Input Output, DVIO, Board is a second source of Digital Video to the MPEG2 Encoder circuit. It is a 1394 IEEE compliant serial input device, sometimes called a Firewire or I link. This kind of output is commonly found on Digital Camcorders.

The Video Input Processor, VIP, receives the selected Analog Video from the Analog Board and the DVIO Board's output. It converts the selected signal to digital Y/UV for recording. The Digital Y/UV is provided to the EMPRESS.

System Clocks

The System Clocks (27MHz) of the Host Decoder, the VSM, the EMPRESS, and the Progressive Scan circuits are generated by an oscillator, 7906. Refer to **Figure 21**. The clock signal is buffered and inverted by 7904, a quad inverter. These signals go to their respective circuits as SYSCLK_XXXX.

The audio clock, ACC_ACLK_OSC is generated by IC7102. During record mode, the audio clock must be synchronized with the incoming Video Field Identifier, VIP_FID. During playback mode, the audio clock, ACC_ACLK_PLL, is generated by the clock synthesizer, IC7900. Both ACC_ACLK_OSC (also goes to the EMPRESS as ACLK_EMP) and ACC_ACLK_PLL are fed to the VSM. The VSM selects the appropriate clock. The EMPRESS IC derives from the incoming ACLK_EMP clock, the I^2S audio encoder Bit clock and Word clock, AE_BCLK and AE_WCLK. They are sent to the VSM with the digital audio.

On/Off

The signal IOn, coming from the Analog Board's microcomputer, enables the switched power supplies. IOn goes Low to turn power On. The switched supplies are: the 3V3, the 5Vdc and 12Vdc on this module.

Reset

Control signal IRESET_DIG, controlled by the microcomputer on the Analog Board is sent to the Reset Logic circuit. The IRESET_DIG transitions to High when the whole system is reset. A Low is output on Pin 1 of 7902. This signal is labeled RESETn. The n on the end of many signal names means enable. The Host Decoder generates several Reset signals after it is operational. the Serial Clock and Data lines provide communication to many of the Microcomputers on the Digital Board.

Audio PLLs

During Playback, the Audio Decoder uses a phase locked clock signal to decode the digital audio, ACC_ACLK_PLL. This signal is generated by 7900. It uses the system oscillator signal that the decoder is using and compares that signal to a feedback signal representing the data coming from the disc, SEL_ACLK1.

During Record, the Audio Encoder and VSM use a phase locked clock signal to Encode the digital audio, ACLK_EMPRESS/ACC_ACLK_OSC. This signal is generated by 7102. It uses the feedback clock signal that the encoder is using and compares that signal to the Field Identifier signal, FID_VIP_FF. This locks the Encoder and the VSM to the vertical sync of the video.

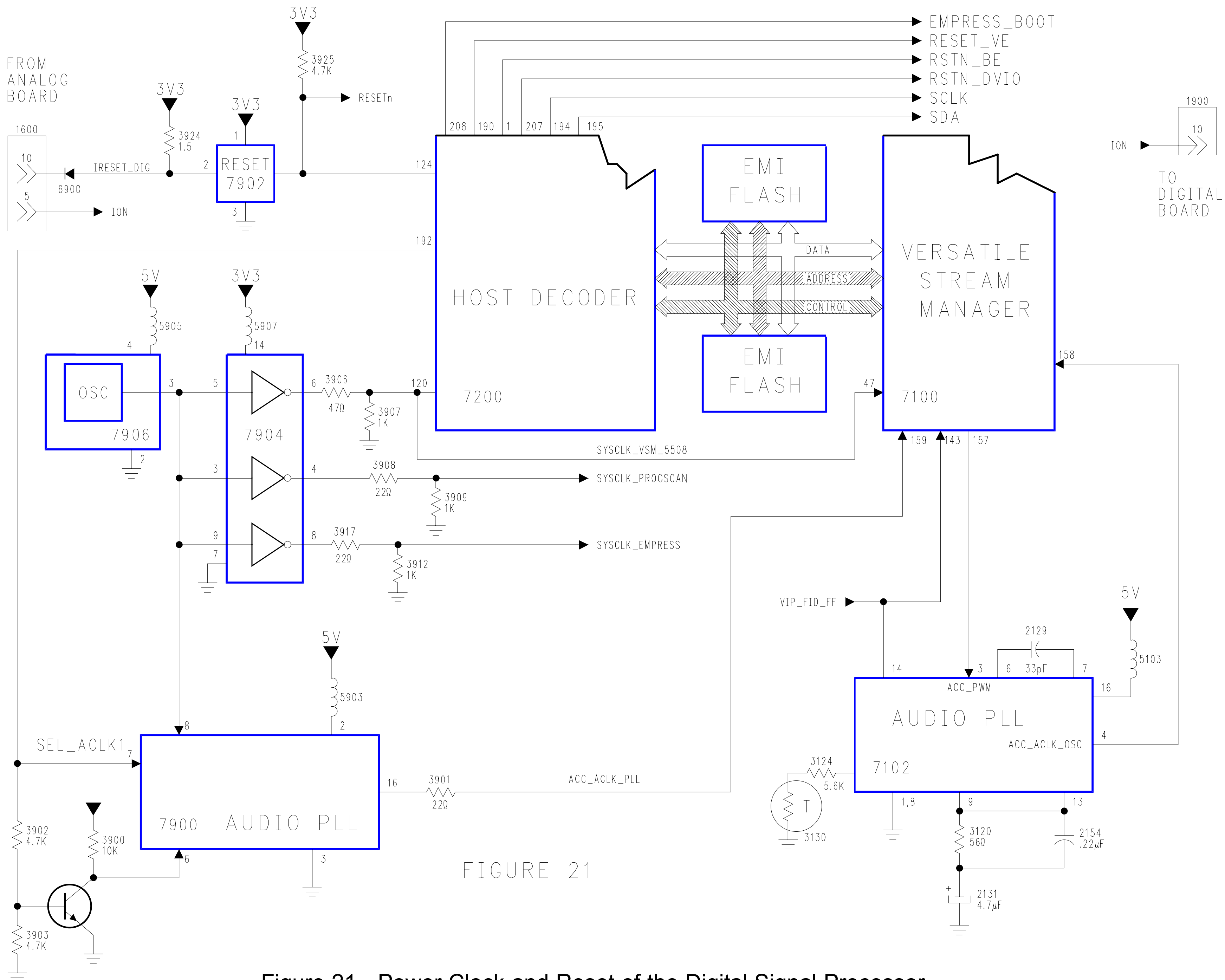


Figure 21 - Power Clock and Reset of the Digital Signal Processor

Video Input Processor

The Video Input Processor Receives the Video input signals, selects one as a source, and converts it to parallel Digital video to be sent to the EMPRESS.

The VIP receives many signal types. Analog Video input signals CVBS, YC, and YUV are routed via the Analog Board to connector 1601 on Pins 14, 16, 18, 20, and 22. The signals are sent to IC7500. If a Digital Video input source is available, 8 Digital Video input signals, DV_IN_DATA (0-7), are sent from the DVIO Board via 1603 to IC7500.

IC7500 converts the Analog Video to Digital Video. The SCLK and SDA control the operation of the VIP. This includes the signal selection.

It then processes the Digital Video to comply with the CCIR656 Digital Video Stream format. The VIP IC selects between the sources and supplies an 8-bit output stream, VIP_Y/UV (0-7). This Digital Video stream goes to IC7403, EMPRESS, and to IC7100, Versatile Stream Manager, VSM. The VSM uses the Digital Video for Vertical Blanking Information, VBI, extraction.

A Field Identifier signal is generated using vertical and a 1/2 V signal using two flip flops. 7504A receives the 1/2 V pulse producing a 1/2V squarewave on Pin 6. This signal is fed to the second FF that is triggered by sync.

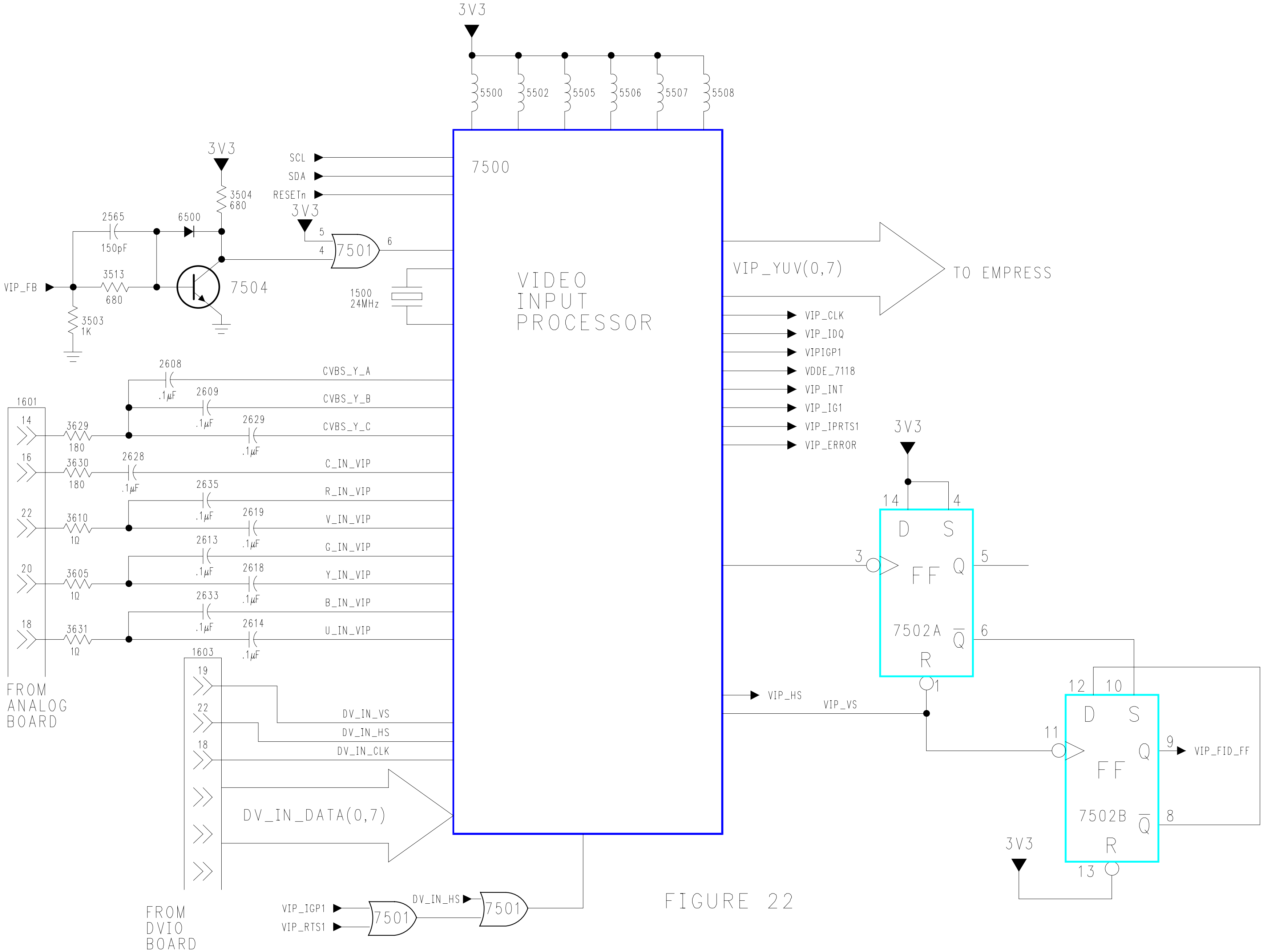


Figure 22 - Video Input Processor

EMPRESS

The EMPRESS IC encodes supplied digital video and audio to be sent to the VSM. The Digital Video stream is converted into an MPEG2 Video stream. Refer to **Figure 23**. I^2S Audio coming from the Analog Board is compressed into a AC3 Audio stream.

The EMPRESS contains a microcomputer. It has a dedicated regulator, 7404. It receives the SYSCLK_EMPRESS as its main clock. It is reset by the RESETn_VE signal. It is controlled by the Host Decoder via the I^2C bus. The EMPRESS uses SDRAM to perform its functions.

Parallel digital video and digital audio are processed by the EMPRESS. 8 bit VIP_YUV comes from the Video input Processor. This is accompanied by support timing signals: VIP_HS, VIP_VS, VIP_IDQ, VIP_FID_FF and VIP_CLK. The Audio Comes in as AE_DATA1, with the WOrd and Bit Clocks, AE_BCLK and AE_WCLK. The Signals are compressed into MPEG2 and AC3. The leave the EMPRESS as VE_DATA and AE_DATA, going to the VSM.

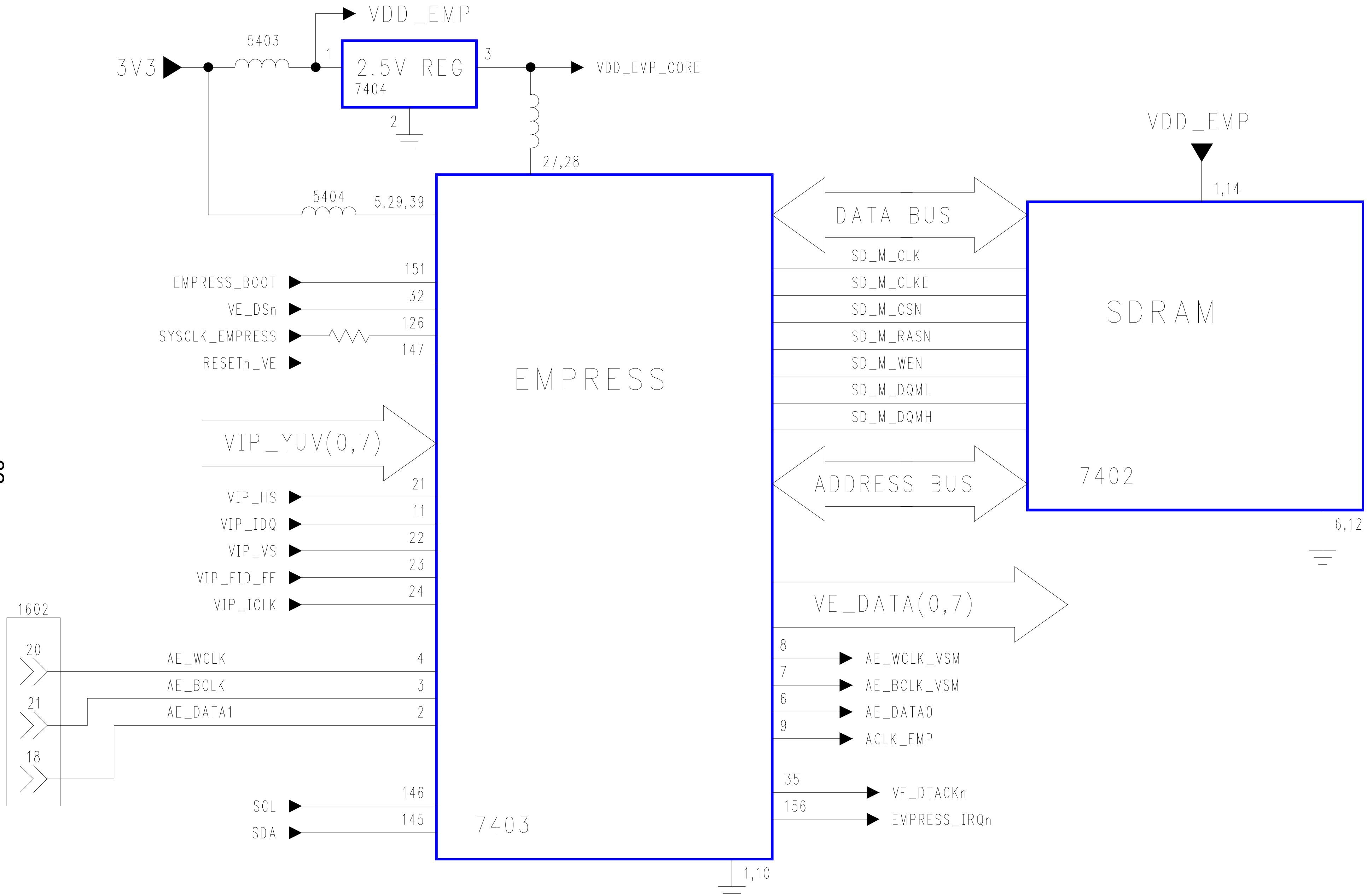


Figure 23 - Empress MPEG 2 Encoder

Versatile Stream Manager

The VSM encodes the Video, MPEG2 and audio, AC3 into a multiplexed I^2S data stream to be recorded on the disc. The I^2S data uses Pins 101-107. It communicates control signals to and from the BE via the S2B bus on pins 24, 132, 154, and 155. It communicates to the System Control Microcomputer on behalf of the entire Digital Board via UART1. It communicates control signals to and from the DVIO Board using UART2. It uses SDRAM to perform its functions. Its boot and operating firmware are in Flash EEPROM of the Extended Memory Interface. It receives its reset using the same signal as the Host Decoder. It also receives the same system clock signal, SYSCLK_VSM_5508.

The VSM must receive data from several sources. The Video comes into the VSM on two data buses. One data bus comes from the VIP, and the other from the EMPRESS. The Video to be recorded is the VE_Data signal lines. MPEG2 has no sync information, so the VIP_YUV signal provides this information for the multiplexing process. The Audio to be recorded comes from the EMPRESS as well. The audio data stream coming in on Pins 177 and 178 uses two special clocks for audio. One is the AE_CLK, and the other is ACC_ACLK_OSC, coming from the Record Audio PLL. The VSM sends to the Host Decoder a Parallel video data bus of multiplexed Audio and Video. This is provided to monitor the Video being recorded.

S2B Interface

The S2B interface between the VSM (IC7100) and the Servo processor MACE3 controls the Basic Engine during record and playback mode. This serial communication goes to the BE on Pins 24, 132, 154, and 155.

Proper operation of the power up sequence involves the VSM. The VSM communicates to the Analog Microcomputer, during the Power Up Self Test operation, using UART1.

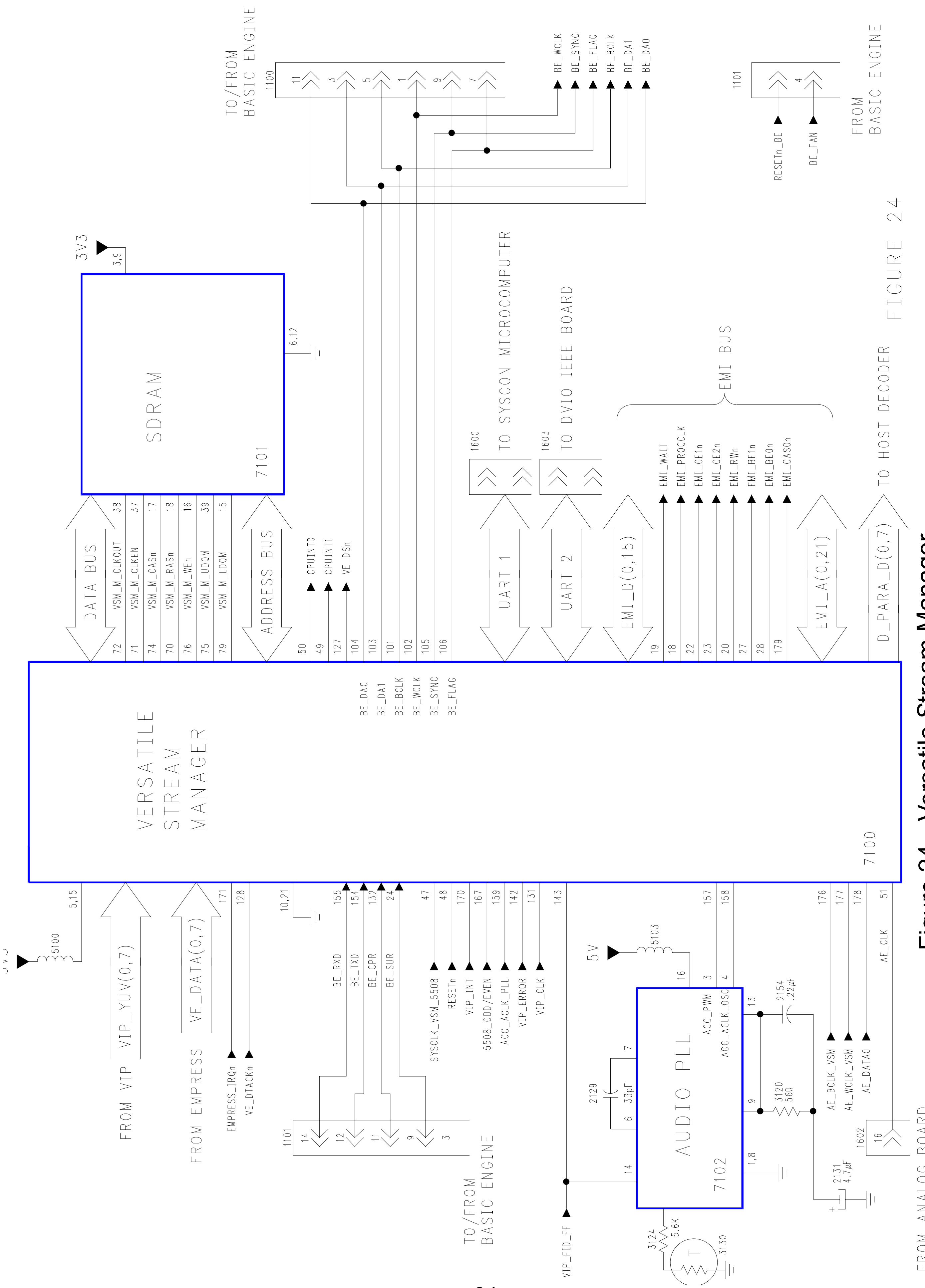


Figure 24 - Versatile Stream Manager

MPEG2 Host Decoder

The Host Decoder has several tasks. It is the Host of the I Squared C Bus for the Digital Board. It participates in the Power up sequence. It performs MPEG2 decoding. It generates the OSD and provides the Service UART serial port. IC7200 uses SDRAM for its many functions. It receives its main clock, SYSCLK_VSM_5508, from 7906 after being inverted and buffered by 7904.

Power On

IC7200 participates in the initialization of the unit. Power up occurs in two stages. 7200 participates in the second stage. After the Analog board and the Front Panel Microcomputer check the unit and pass their tests, the Analog Microcomputer turns On the Standby supplies. It uses an ION control voltage that passes through the Digital Board. This includes the 3.3Vdc supply for 7200. 7200 then receives the DIG_Resetn signal from the Analog Board.

7200 creates reset outputs for the Digital Board, the DVIO Board and the BE: Resetn_VE goes to the EMPRESS. RSTN_DVIO goes to the DVIO Board. RSTN_BE goes to the BE. The EMPRESS_BOOT signal goes to the EMPRESS for its start up flag. The Decoder is a 2.5Vdc device. The BE and the DVIO microcomputers are 3.3Vdc devices. 7702 elevates the reset signals to 3.3Vdc.

If 7200 passes its self test and the other ICs communicate properly, the unit's power will stay On. If not, the unit will go into Sleep mode, never looking for keyboard input again. This process has 10 Seconds to occur. If it does not, the Analog Microcomputer will place the unit in sleep mode, turning Off the Standby supplies which is the VCC for most of the ICs on the Digital Board.

Playback

During playback, the serial data from the Basic Engine goes directly to the MPEG2/AC3 Decoder, IC7200. The serial Front End I^2S Interface receives the signal on Pins 17-22. Refer to **Figure 25**. The A/V Demultiplexes, separates the Audio and Video data. IC7200 then decodes the MPEG2 video and AC3 audio. It contains the analog Video Encoder and has the following outputs to the Analog Board: RGB, Y/C, CVBS, I^2S Audio, (PCM format) and SPDIF Audio (Digital Audio output).

There is another video output path from IC7200. The Digital Video for the progressive scan circuit, PSCAN_YUV(0-7).

Record

It receives the Parallel Video output of the VSM. The Parallel Video path sends the recordable video and audio back to the outputs during record and powered up standby. It receives the selected Multiplexed Data stream from the VSM via the D_PAR_D(0,7) lines. There are support signals for the Parallel Data Stream on Pins 196, 201, 205, and 206. Because of the amount of processing, the output video at the rear jacks is delayed about 4 seconds from the video coming into the unit.

ComPair

The ComPair service aid connects to 7200 via a serial communication port. Using ComPair software and a computer, service troubleshooting and adjustments can be performed.
ComPair has a dedicated connection on the Digital Board, 1901. The input Pins for 7200 are 2, 3, 197, 200, and, 204. ComPair cannot function if 7200 does not initialize properly. The port's inputs and outputs are buffered by 7905.

EMI

The Extended Memory Interface is used by the VSM and the Decoder. It is Flash EEPROM. It contains the boot and operating firmware for the VSM and the Decoder. Like all other memory, it uses an address Bus, a Data Bus, and support control signals.

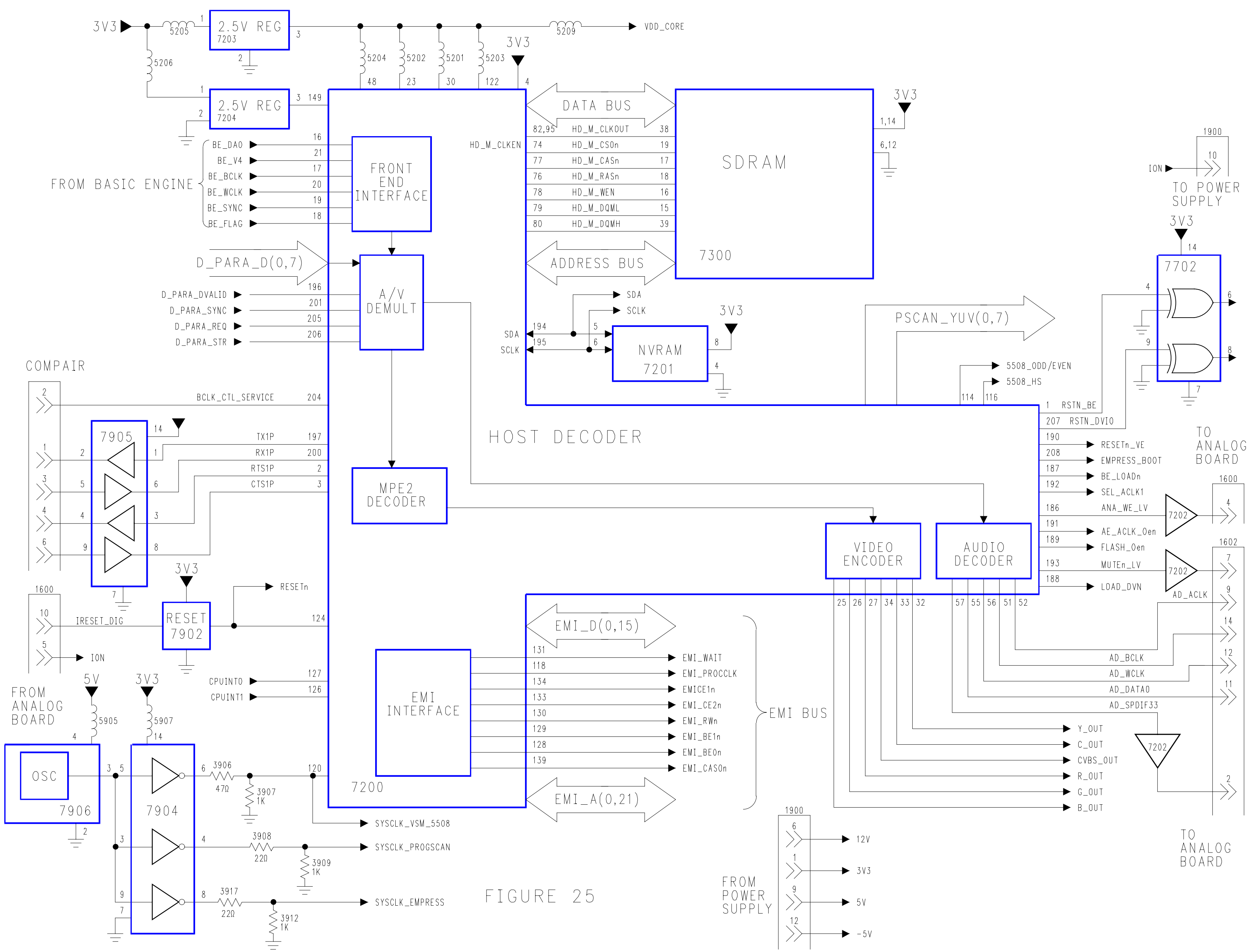


Figure 25 - MPEG2/AC-3 Decoder Circuit

Progressive Scan

The progressive scan section is integrated into the Digital Board and built around the SAGE Fli2200 Deinterlacer/Line Doubler (7700). Refer to **Figure 26**. This I^2C controlled device uses 64Mbit SDRAM (32bit x 2M) to perform high quality Line Doubling, or de-interlacing (meshing). The Line Doubler gets Digital Y/UV input data on Pins 20-27, from 7200. The format of the Digital Y/UV input is CCIR656 with separated H sync, V Sync.

Because IC 7200 doesn't have a V sync output, the odd/even output of this IC has to be translated to a V sync signal. Vertical sync is generated with a flip-flop IC7701 and an XOR, 7702.

Power and Clocks
IC7700 uses two supplies, 3.3Vdc and 2.5Vdc. The system clock, SYSCLK_PROGSCAN, is running at 27Mhz.

7700 produces three 10-bit output signals, Y, Cr and Cb. These are sent to the D/A converter 7801.

D/A Digital Encoder

The output of 7701 (4:4:4 progressive Video) is fed to the Digital to Analog Device, 7801. The RGB output is a current signal fed via a low pass filter to the output Op Amps, 7802 and 7803. The Analog Video, 480P, is fed via a 7-conductor flex cable to the Analog Board.

Power and Clocks
IC7801 uses the 3.3Vdc supply. The system clock, SYSCLK_PROGSCAN is running at 27MHz.

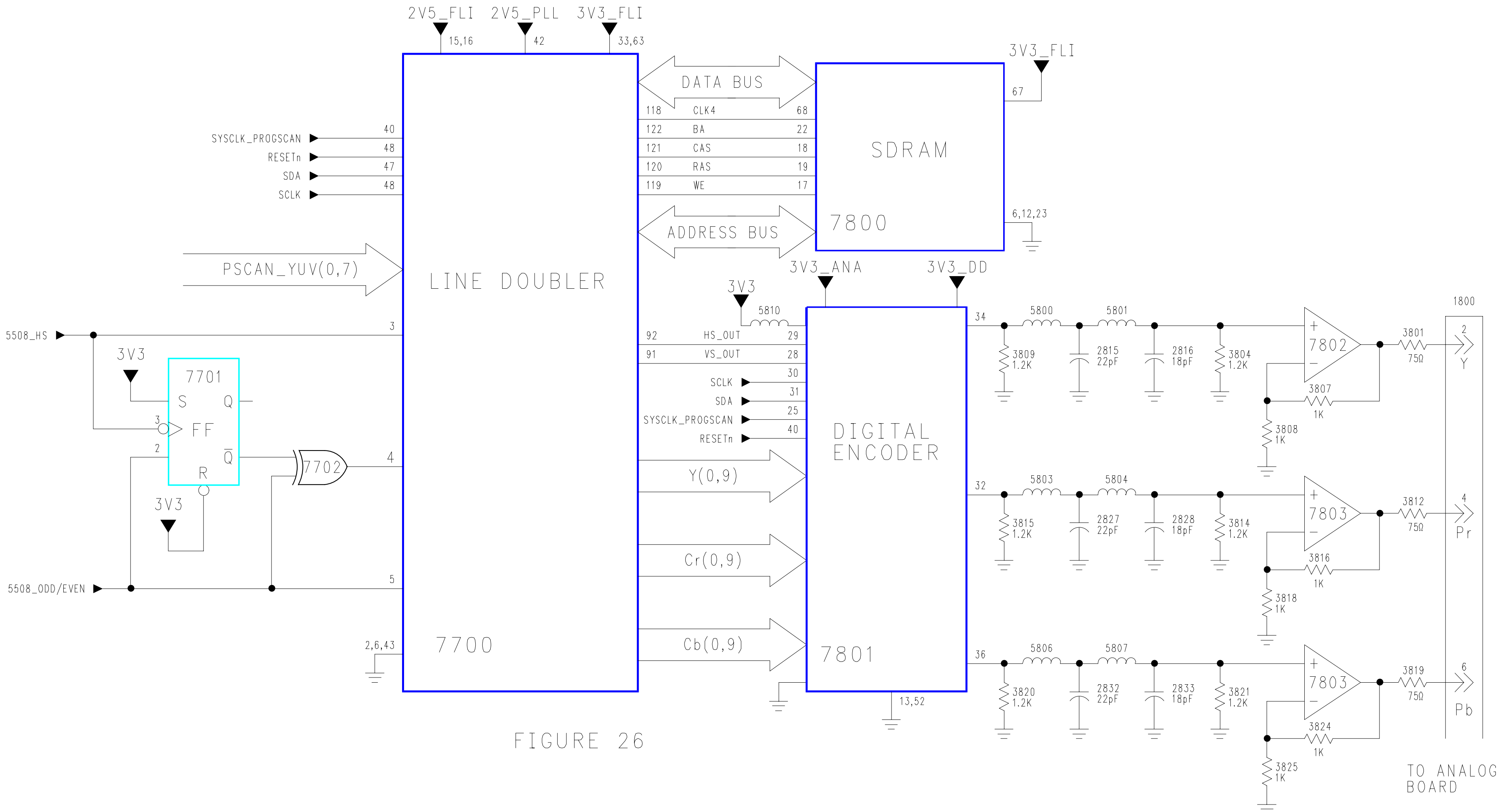


Figure 26 - Progressive Scan

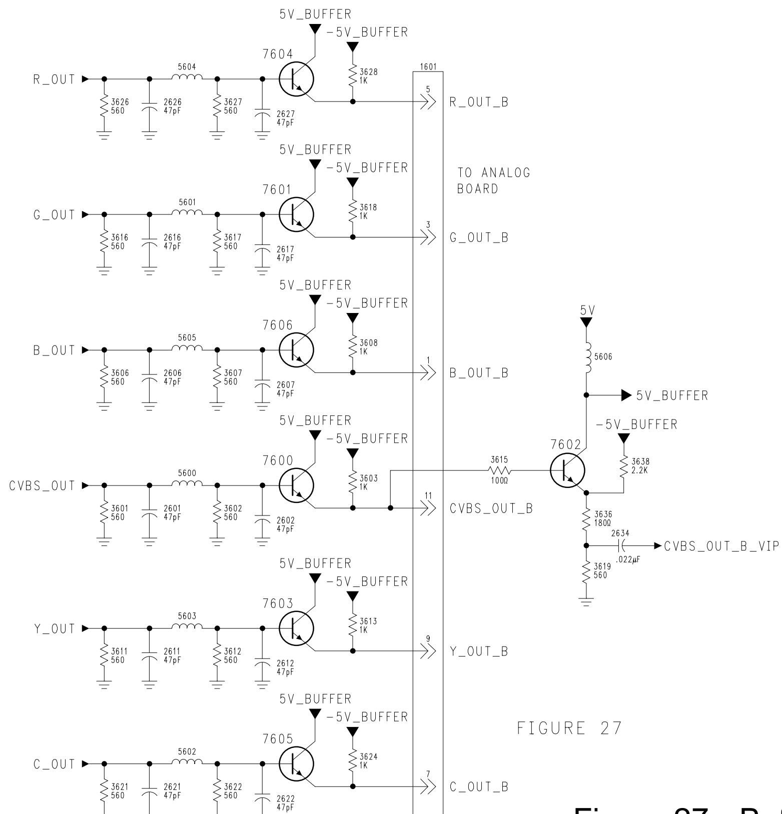


Figure 27 - Buffers

Digital Signal Processor VN04

The functionality of the two Digital Boards is Identical. Refer to **Figure 28**. It is responsible for encoding Digital Video and Audio into MPEG2 and AC3 respectively. It supplies MPEG2 and AC3 via an I squared S serial protocol to the Basic Engine (BE) for recording. It also receives the MPEG2 Video via I^2S from the BE, decodes the signal, and supplies Digital Video to the Progressive Scan circuit. It supplies Analog Video to the Analog Board, and Digital Audio (I^2S) to the Analog Board. The DVIO Board's circuitry has been migrated to the Digital Board.

Most of the Digital Board's operations are centralized into one microcomputer, 7400. It uses two DRAM ICs to perform its functions. 7400 uses Flash EEPROM to store its firmware. It performs MPEG2 encoding. It combines the Audio and Video into one data stream. It communicates control signals to the BE. The Digital Video/Audio Data is sent back through the playback signal path. It perform MPEG Decoding and analog signal generation. It produces an 8-bit digital Y/UV for the Progressive Scan circuit. It produces two types of Audio, I^2S and SPDIF. They both go to the Analog Board.

The Progressive Scan, Pscan, circuit, 7703 sends Y/Pr/Pb analog, 480P, Video to the Analog Board to be provided to the output jacks. The Pscan circuit contains a Line Doubler and a Digital Encoder. The Line Doubler receives the 8-bit Y/UV from 7400. It doubles the vertical scan lines and produces separate Y, Pr, and Pb. The signals are passed through amplifiers before they are sent to the Analog Board.

The Video Input Processor receives the selected input signals from the Analog Board. It has two major functions. It performa A to D conversion and Serial to Parallel conversion. it provides 8 Bit Digital Y/UV to the Microcomputer.
The Digital Video Input Output, DVIO, Board is eliminated using the VN04 Digital Board. The Microcomputer performs most of the signal processing. The Physical and Link circuits work the same as the previous DVIO. It is a 1394 IEEE compliant serial input device, sometimes called a Firewire or I link. This kind of output is commonly found on Digital Camcorders.

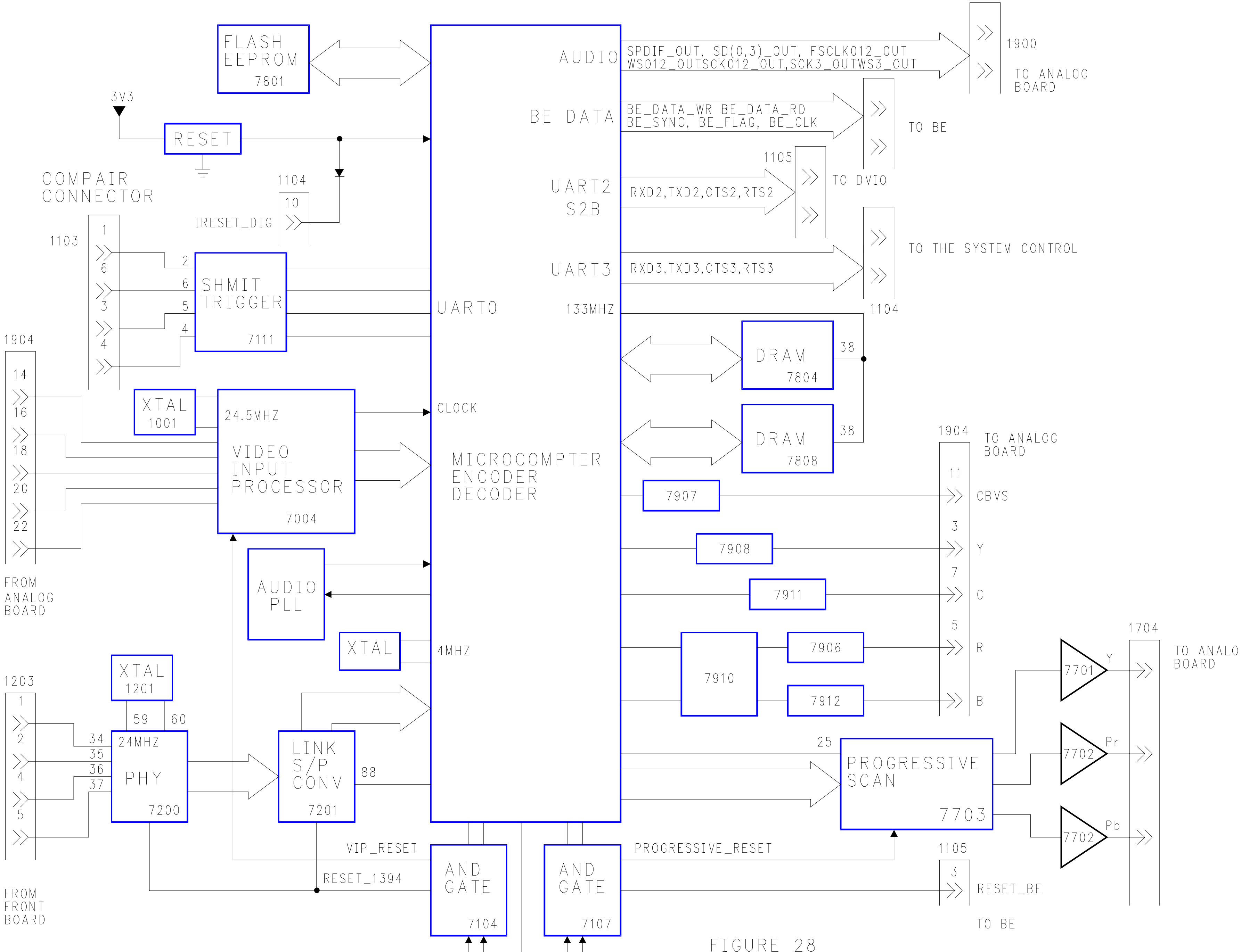


Figure 28 - VN04 Digital Board

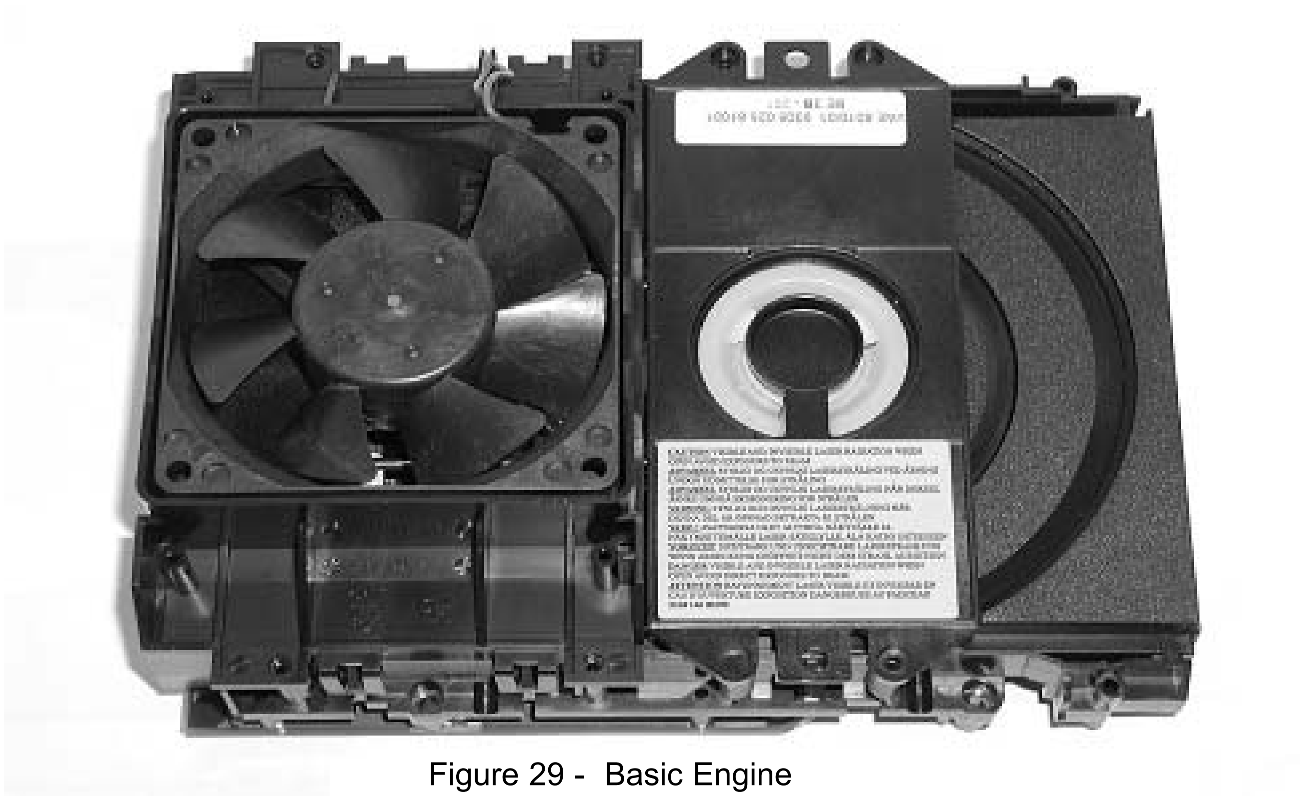


Figure 29 - Basic Engine

DVD Mechanism and Servo Board

Basic Engine

The Basic Engine consists of a DVD-Mechanism with dual laser Optical Pickup Unit (OPU), a tray loader, a fan unit, and a PCB containing all electronics to control the module. The OPU contains the Focus and Radial Motors. The Mechanism holding the OPU contains the Sled and the Tilt Motors. The electronics of the module are responsible for all the basic servo tasks. It reads and writes data to and from the disc.

The PCB is multilayer, using Surface Mounted Circuitry with a very high component density. Detailed diagnostics and fault finding are available via ComPair.

Some specifications:

* Record DVD+R and R/W
* Lossless linking
* Recording speed: 1.2 x
* Playback DVD, DVD+R(W), DVD (SL/DL), DVD-R, DVD-RW (V1.1)
* Playback speed: 1.2 x
* Playback CD, CD-DA, CD-R, CD-RW, CD-ROM, VCD/SVCD
* Playback speed: 3 x
* It controls all other functions like tray control, start/stop, disc rotation, tracking, jumping, and communication to the Digital Board.

The Servo circuit provides the interface between the Mechanism and the Digital Signal Processing Board. It is mostly on one board attached to the bottom of the mechanism. It is made up of four main circuits:

* The SPIDRE is the Signal Processor IC for DVD Recordable
* The MACE3 is the Mini All in one CD Engine third generation.
* The Encoder/Decoder is the Translation circuit for data going to and from the disc.
* The AWSOME is the Adip Decoding, Wobble Proccessing, Error Correction, Synchronous start Stop and Occasionally Mend Errors.

Initialization process
During power-up, a reset of the BE is preformed. This is parallel to the reset process of the Digital Board. After the MACE3 resets, a System reset

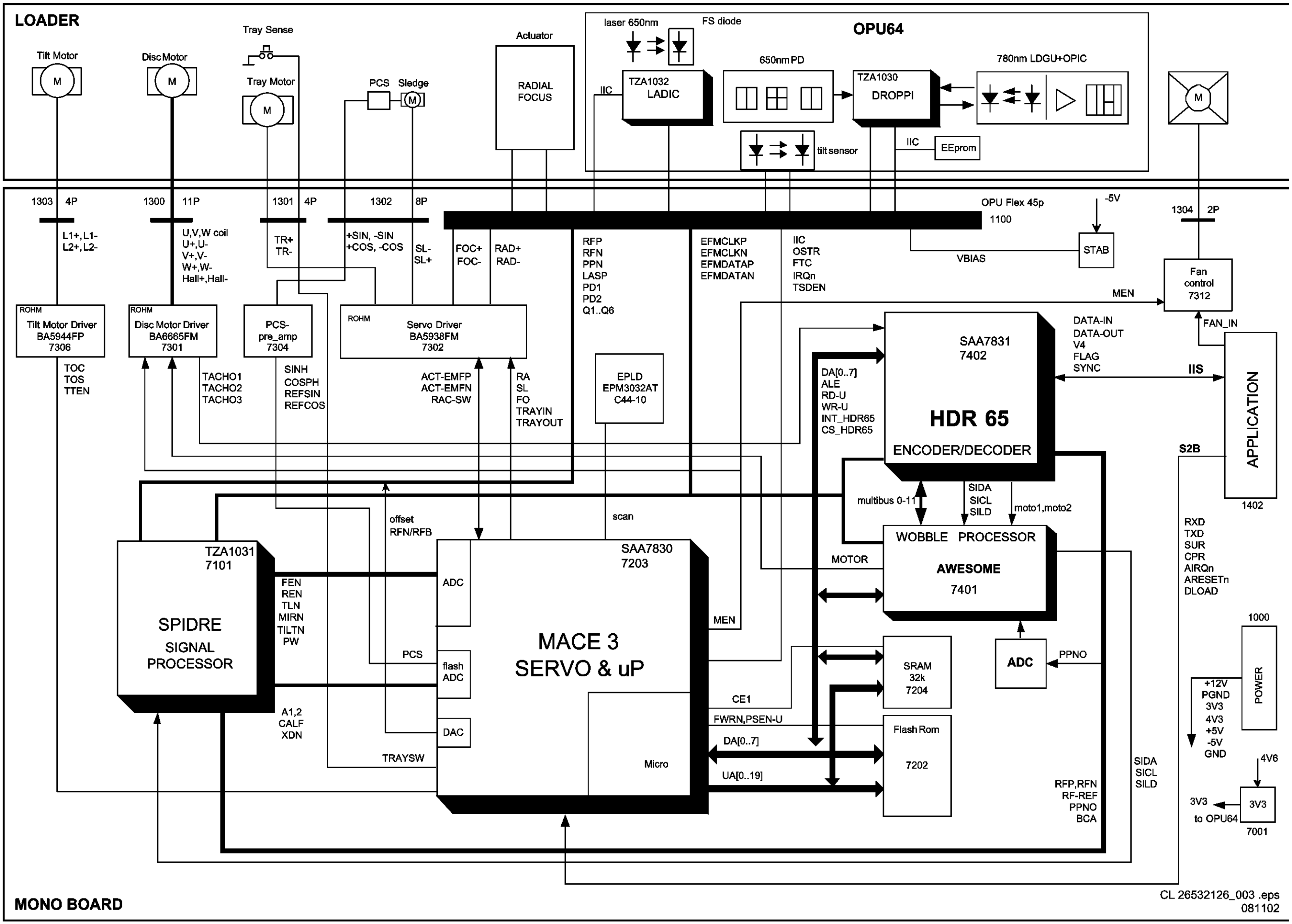


Figure 30 - Servo Block Diagram

occurs to reset the other microcomputers in the BE. A self-test will automatically start. Each of the microcomputers must respond to the I^2C bus. The SDRAM and flash are also tested. If the self test passes, the SUR signal line will go Low. Part of the self test is the CPR switching voltage coming from the Versatile Stream Manager. If it is ready to function, it will be Low. After the self test passes, the BE will wait for the first Serial to Basic Engine, S2B, user command. E.g. "Tray_out".

Disc recognition process
The process of disc recognition is entirely performed within the BE. If the disc is not recognized, the problem is in the BE or something missing supplied to the BE. Information about the disc type is sent via the Subcode data path to the MPEG2 Decoder microcomputer.

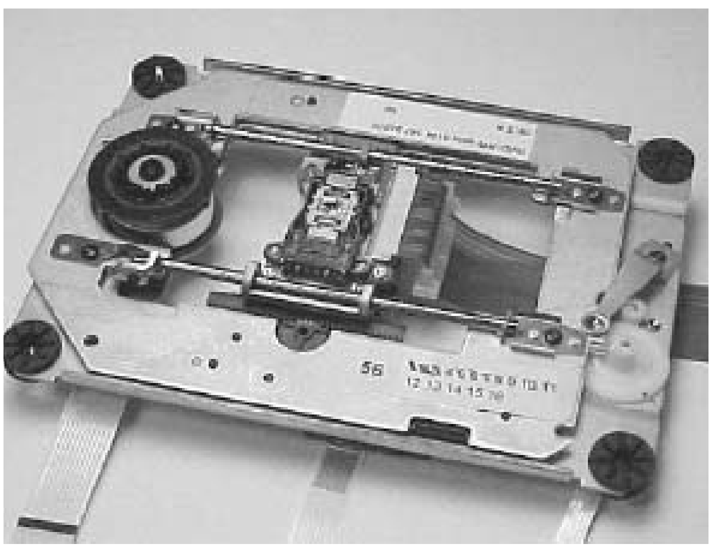


Figure 31 - DVDM

DVDR Mechanism

The DVDR-M is made up of three components: Optical Pickup Unit, OPU, the Sled, and the Turntable Motor. The OPU contains two lasers: one for CDs with a wavelength of 780 nm, and one for DVDs with a wavelength of 650 nm.

The OPU contains: the Optics, the Focus Motor, the Laser Drive IC (LADIC), the Tilt sensor, the DVD Rewritable OPU Pre-Processor IC (DROPPI), and the EEPROM with the OPU adjustment data.

DROPPI

The DROPPI (DVD Rewritable OPU Pre-processor IC) is a multi-purpose analog pre-processor. It supports many photo detector configurations and output signal modes. It produces RF and servo feedback signals, Q1-Q6. Its output signals are on the same flex ribbon cable with the wideband RF (differential signals). The Wobble, focus, and Sled Servo signals are relatively low bandwidth.

LADIC

The Laser Drive IC, LADIC, controls the data to the lasers, and the supply to them. It performs three main functions:

· It drives the laser for both playback and record functions. Its greatest stress is realized during record, producing data signals and write pulses. The recording process is flexible with respect to the input modulation method (EFM, EFM+, 17 pp, etc.). This is necessary to support CDR/RW and DVDR/RW. To accomplish this, the LADIC uses two Random Access Memories (RAM) which can be loaded (non real-time) via the I^2C Bus from the microcontroller.

· It drives the laser with a sequence of programmable write pulses with high timing accuracy and high peak current levels.

· It controls the exact light power levels coming from the laser and controls the exact power absorbed by the disc during recording.

The LADIC needs three independent power supplies. These are the analog and digital power supplies, and V Bias for the laser driver function. The supplies are separate to obtain maximum output performance where there are large and highly dynamic current flows.
The LADIC is controlled by an I^2C bus. The laser is operated at three current levels: Playback, Record and Erase. During the initialization of a disc to be recorded on, and test recording is performed in a special place on the

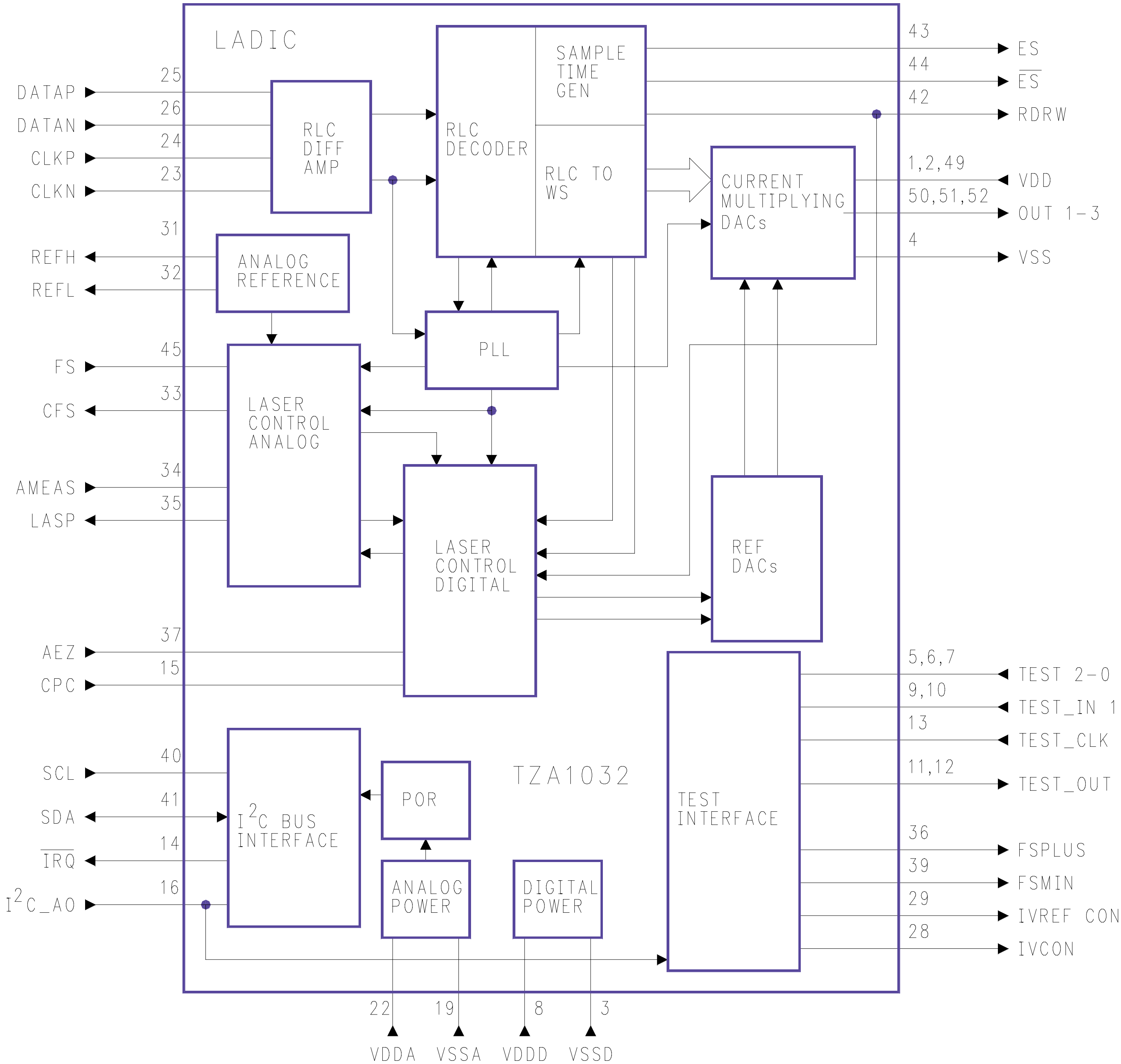


Figure 32 - Laser Drive IC

innermost section of the disc. A series of random data is recorded with a wide range of current levels. The data is played back. Two feedback signals are generated and sent to the MACE3 circuit, A1 and A2. A second Fine tuning of the Optimal Laser Current is performed. The disc is written to again except the current range is chosen by the MACE3 using the feedback received. This fine tuning of the laser current produces the Calf feedback signal that is sent to the MACE3 and it is stored in the MACE3's operating RAM.

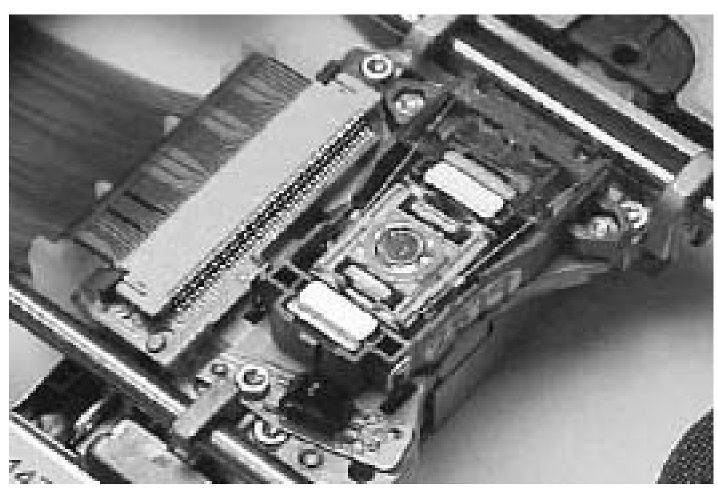


Figure 33 - OPU

Servo Circuit Description

The Servo circuit provides the interface between the Mechanism and the Digital Signal Processing Board. It is mostly on one board attached to the bottom of the mechanism. It is made up of four main circuits:

The SPIDRE
The MACE3
The Encoder/Decoder
The AWSOME.

Servo Power and Reset
The Servo receives: 12Vdc, 5Vdc, 3.3Vdc and -5Vdc from the Power Supply. There are three 2.5V supplies on the Servo Board connected to the 3.3Vdc supply. The MACE3 is reset by the Digital Board, via the Reset_BE signal. A Reset signal comes from the MACE 3 for the rest of the servo. The Mace3 is the Host for the local I^2C Bus.

SPIDRE

The SPIDRE (Signal Processing IC for DVD REwritable) is a multi-purpose analog pre-processor IC specifically intended for writing applications.

The SPIDRE receives two Power Supplies: -5Vdc and 5Vdc. Its has three main tasks. One is to interface the Servo signals that go to the MACE3 Servo Processor. The Second is Preprocessor for the RF signal coming from the disc during playback. The third is to process the RF signal coming from the Encoder during record.

The SPIDRE is controlled by the AWSOME via a serial bus on Pins 35, 37, and 38. The AWSOME communicates: gain information, data type, and operation mode, Play or record.

The Servo signals to be processed include: Playback HF/RF, the focus servo feedback signals, the radial feedback, the track loss signal, and tilt sensor signal. The HF/RF (EMF) signal varies greatly between disc formats. The Focus Error and Radial Error signals come from the mechanism on the Q1-6 signal paths. The Tilt Error has a Photo Tilt Sensor. The dynamic range of these signals is very large. They are converted to Lower frequency RF data paths that the MACE3 can accommodate. This is required for playability of the many different kinds of discs.The error signals are all balanced to reduce noise interference. Thus, they are named XX positive, and XX negative. The Output signals include: the Focus Error, the Radial Error, the Tilt error, laser Power, and tracking loss signals.

The Record RF EFM data and EFM Clock comes from IC 7402, Encoder circuit, and is supplied to the SPIDRE on Pins 48-51 of 7101. The SPIDRE processes the RF signals for gain control of the Error control signals going to the MACE3 during record. All of these signals are balanced. Thus there is a negative and a positive signal for all of them.

The LASP, Laser Power feedback signal is processed by the SPIDRE. During playback, the EFM coming from the disc is used by the ALFA circuit to generate the AMEAS, ALFA Measurement signal that goes back to the LADIC for precise control of the LASER power. During record, the EFM signal coming from the Encoder is used by the ALFA circuit to create the AMEAS signal.

The pregroove tracking error signal comes from a Preprocessor in the OPU. The PPN signal is amplified and sent to the Wobble Processor in the Decoder circuit.

PRE-PROCESSOR

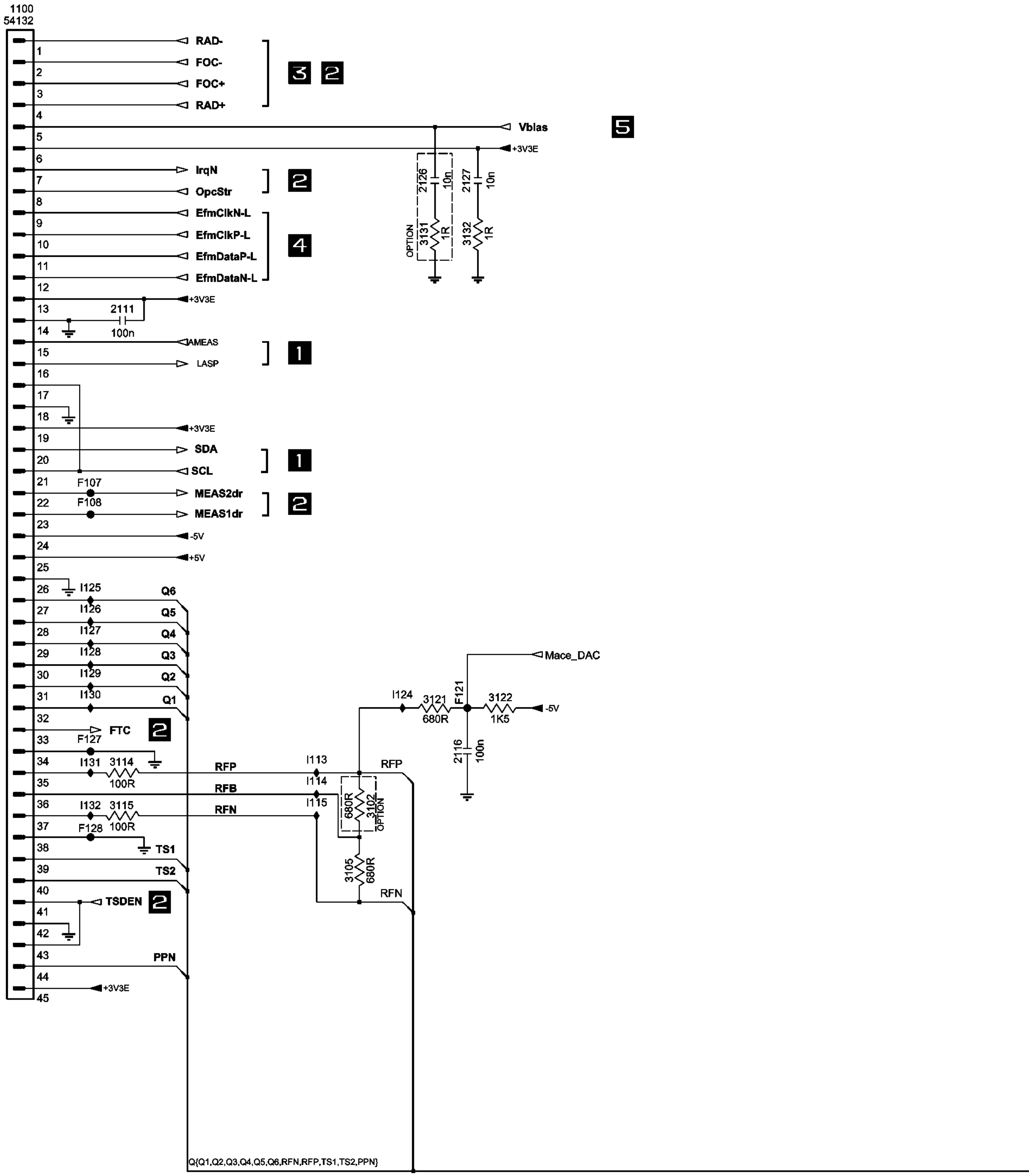
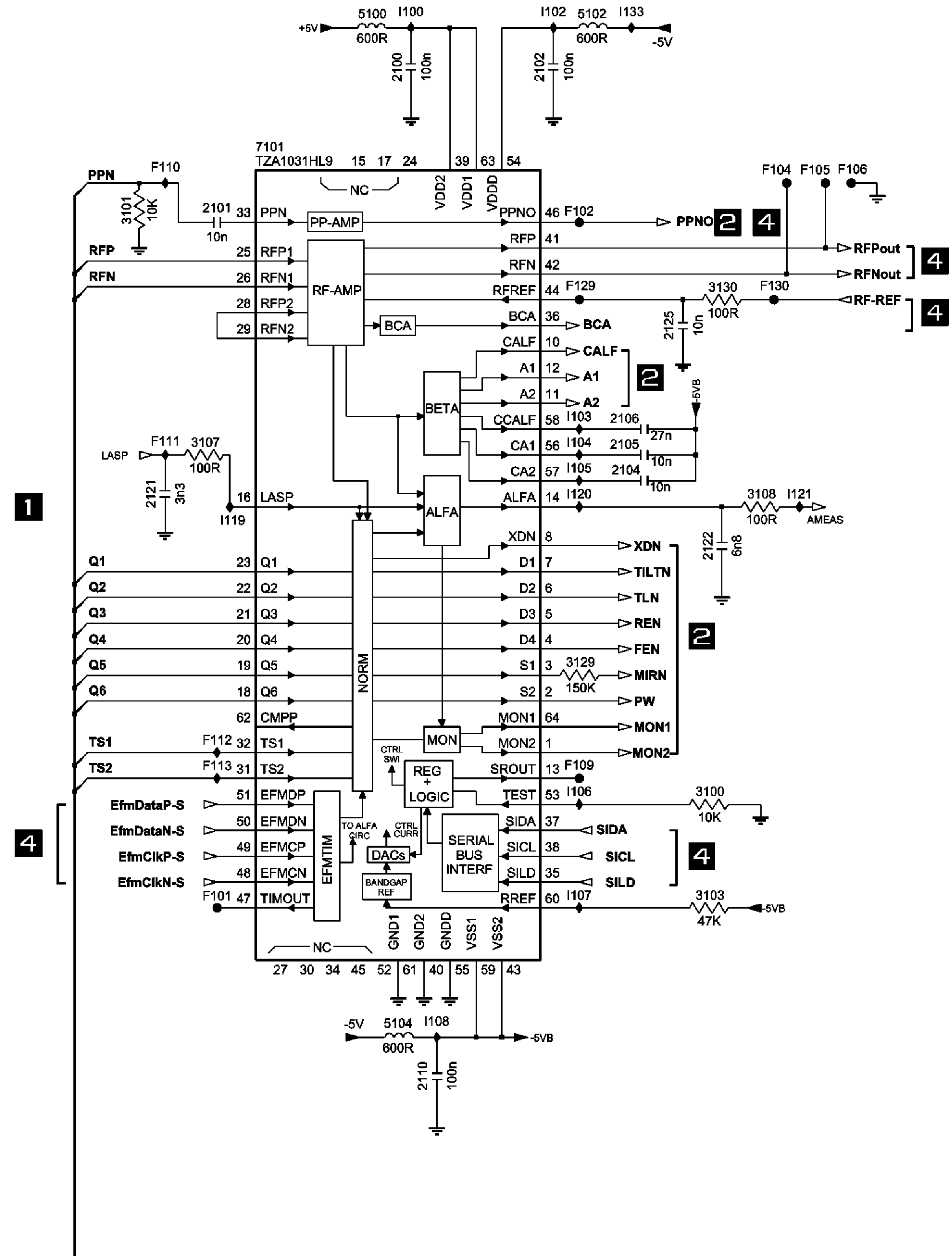


Figure 34



- PRE- Processor

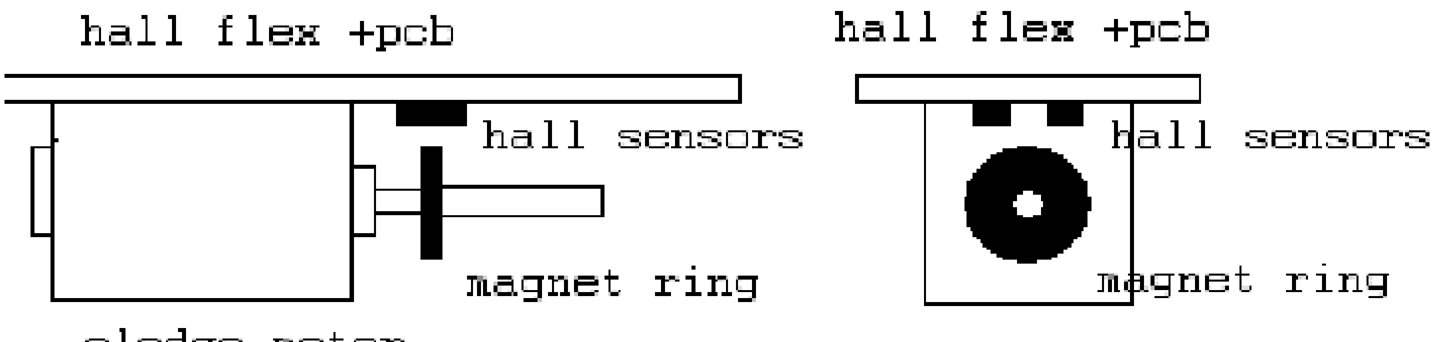


Figure 35 - PCS Motor

MACE3 Servo Microcomputer

The MACE3 IC is the Mini All Cd Engine third generation. Its vendor number is SAA7830. It is a combined servo processor and microcomputer. The servo processor handles the signals for focusing and tracking for disc access. It also generates the control signals for tray control. In a CD/DVD system, there are several active control loops. Some of them are needed to adjust the servo error signals. It monitors and adjusts the offsets, signal amplitudes, and loop gains (AGCs). The control loops determine the laser spot position on the disc in the radial (Sled),

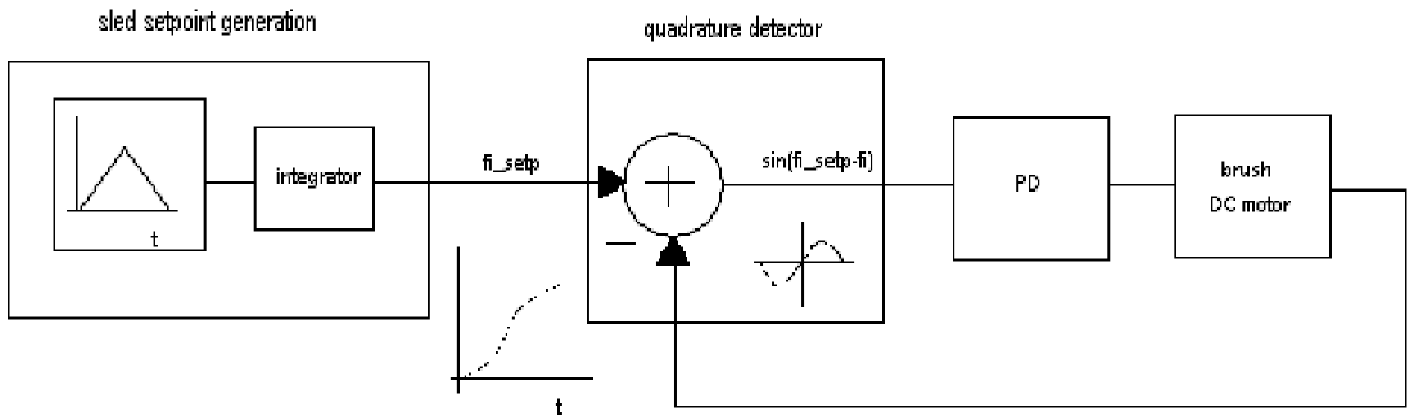


Figure 36 - PCS Phase comparison

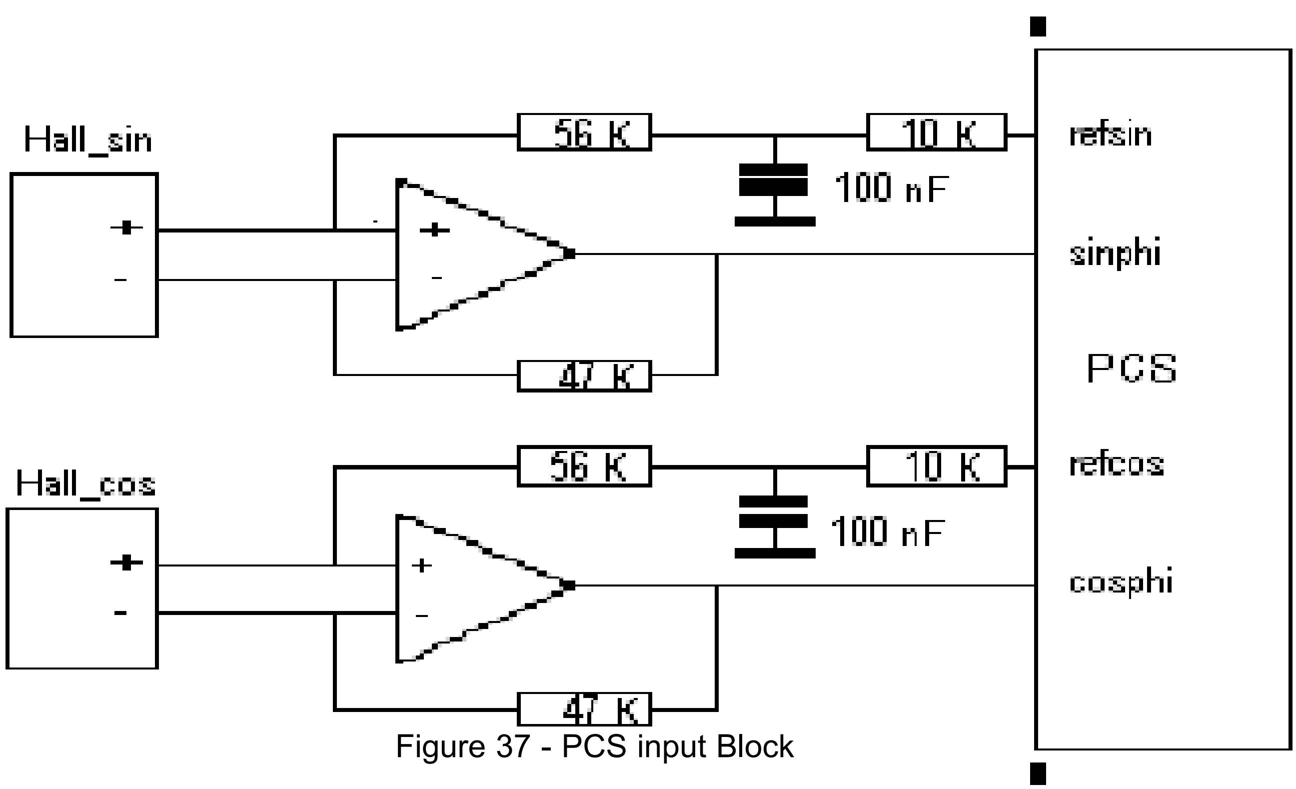


Figure 37 - PCS input Block

axial (focus), and tangential directions (Tilt). This access system consists of two parts, namely the Focus Actuator and the Sled, which are, within a certain range, mechanically and electrically independent.

The analog signals from the SPIDRE are converted into a digital representation using A/D converters. The digital codes are then applied to logic circuitry to obtain the various control signals.

OPC (Optimum Power Calibration)
This device has an integrated Optimum Power Calculation block for use in CDR, CD-RW, and DVD+R applications. It reads three analog signals: A1, A2, and CALF. These represent Max, Min, and Average values of the EFM coming from the disc, respectively. It also takes the Power (PW) signal from the laser controller and then feeds an analog signal, ALPHA0, out to control the laser power. The conversion frequency is 88kHz per channel. Basically, the OPC procedure tries to find out the optimum laser power to be used on a specific disc. It consists of three phases:

1. WRITE - Random EFM data is written to the test area of the disc at increasing levels of laser power, controlled by ALPHA0.

2. READ - The data on A1, A2, and CALF is read back from the test area and stored in memory.

3. CALCULATION - the embedded microcomputer then calculates the setting of ALPHA0 where the least jitter is encountered. Some pre-processing is carried out by the OPC logic to reduce the processor's load. This sequence is performed twice - first a coarse calibration, followed by a fine-tuning.

The micro controller has many responsibilities. It processes the Serial to Basic Engine, S2B, commands from the Digital Board. It controls the various processes in the mechanism via I^2C.

The MACE3 uses a Parallel communication bus for access to its Flash ROM. Refer to **Figure 38**. The Flash Memory contains the firmware for the BE. The MACE3, the Encoder and AWSOME share a parallel bus with 32K of SRAM

When the power is applied to the unit, the Digital Board sends a reset signal to the MACE3. The MACE 3 checks its SRAM, then reads its Flash Rom and sends a System Reset signal to the ICs on the Servo Board. When its memory tests are complete and they pass, a SUR control voltage goes low, indicating to the Digital Board that it is ready to receive commands. It then initializes its I Square C Bus and communicates to the DROPPI and LADIC on the Mechanism. The Tilt Motor is exercised and centered. The PSEN signal then appears.

The Microcomputer produces several outputs. Many of them are error signals. It produces: the Radial Error, the Focus Error, the Tilt Motor control, and the Position Control Sled (PCS) signals. Each of the motors has a driver circuit.

The Microcomputer controls the Tray motor drive circuit. The Tray switch goes directly to the MACE3.

The Microcomputer controls the PCS. The Position Control Sled must operate very accurately. It cannot track the Disc’s tracks of 1.6 microns alone, but its precision is a must. There are two Hall sensors positioned 90 degrees apart in a circular fashion. A round magnet is attached to the armature of the drive motor. The positioning of the sensors gives them their name, Sine and Cosine. The motor is a basic universal type. The exact rotation of the armature is detected by the Hall Sensors. The phase of the Hall sensor signals are compared to a reference signal generated internally by the MACE3. The focus actuator moves the lens side to side for tracking the individual tracks. When the drive current to the actuator increases to a certain point, the microcomputer knows the Sled must be moved. The Sled is driven to minimize the actuator’s drive current, meaning it is right under the proper track. The microcomputer produces the Reference DC offset for the Op amp inputs.

2 MACE3

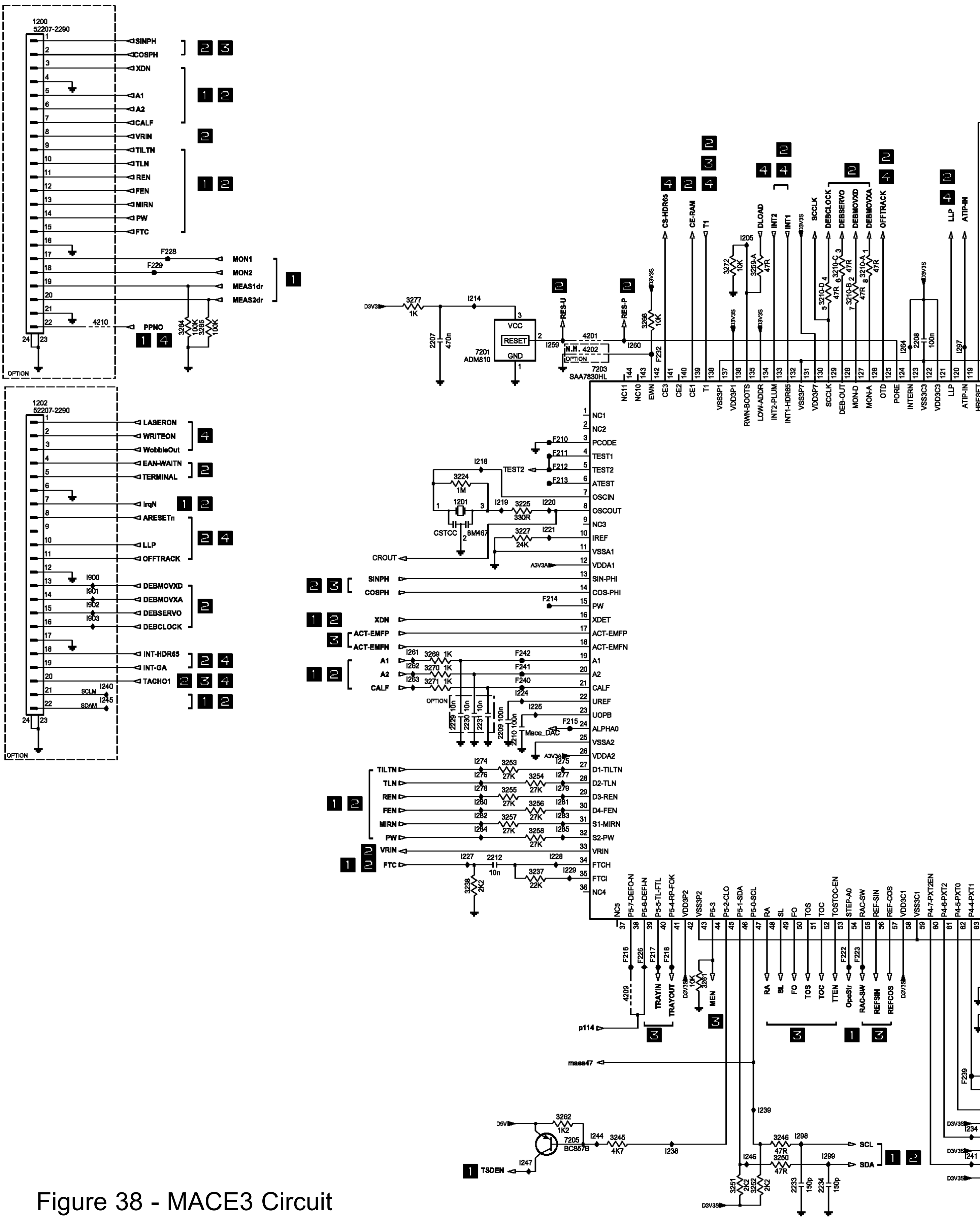
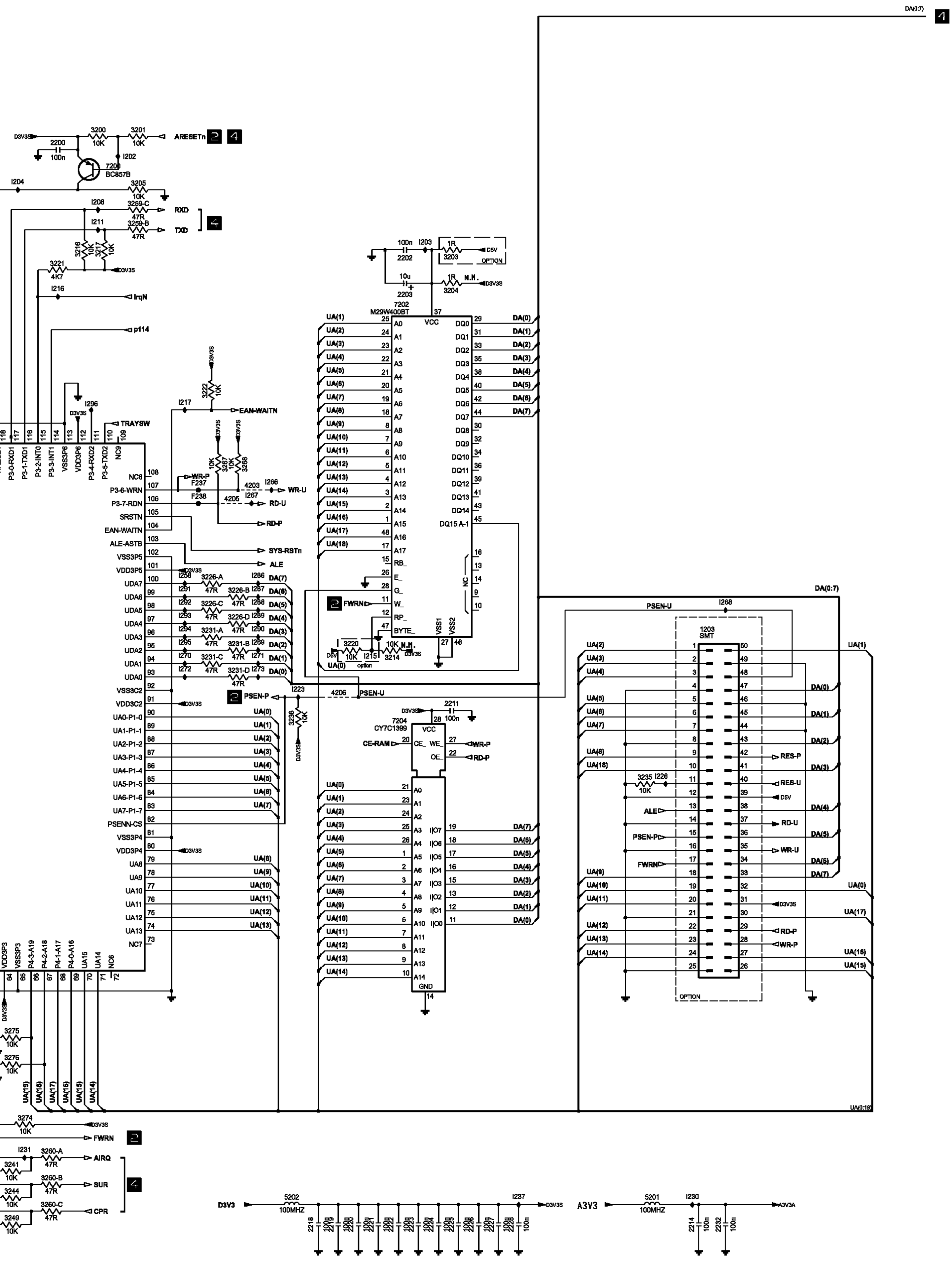


Figure 38 - MACE3 Circuit



DA(0:7)
ARESETn
RXD
TXD
IrqN
p114
TRAYSW
EAN-WAITN
WR-P
WR-U
RD-U
RD-P
SYS-RSTn
ALE
PSEN-P
PSEN-U
FWRN
7202
M29W400BT
VCC
VSS1
VSS2
7204
CY7C1399
CE-RAM
1203
SMT
OPTION
RES-P
RES-U
D5V
D3V3S
AIRQ
SUR
CPR
D3V3
5202
100MHZ
A3V3
5201
A3V3A
UA(0:19)
7200
BC857B
P3-6-WRN
P3-7-RDN
SRSTN
EAN-WAITN
ALE-ASTB
VSS3P5
VDD3P5
PSENN-CS
VSS3C2
VDD3C2
VSS3P4
VDD3P4

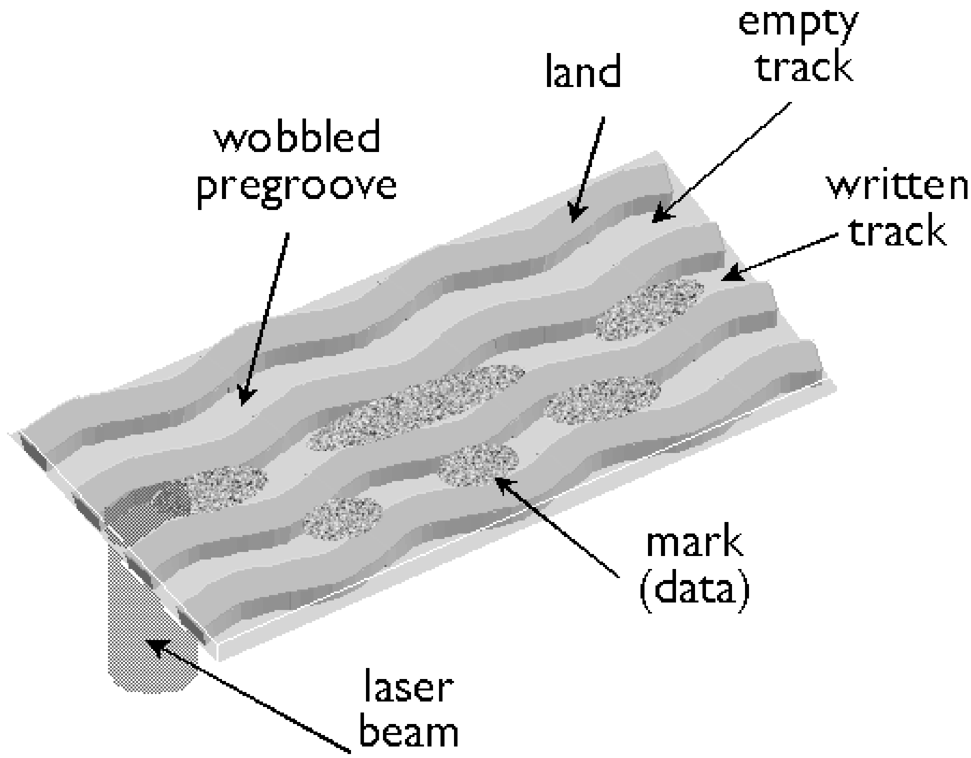


Figure 27 - Wobble Tracks

Wobble

A Pre-groove is stamped on writable discs. All recordable DVD media types feature a microscopic wobble groove embedded in the plastic substrate. This wobble provides the recorder with the timing information needed to place the data accurately on the disc. During recording, the drive's laser follows this groove to ensure consistent spacing of data in a spiral track. The walls of the groove are modulated in a consistent sinusoidal pattern, so the Wobble processor can read and compare it to an oscillator for precise rotation of the disc. This modulated pattern is called a wobble groove because the walls of the groove appear to wobble from side to side. This signal is only used during recording, and therefore has no effect on the playback process. Among the DVD family of formats, only recordable media use wobble grooves.

Lossless linking describes the need to connect data streams on a disc without any unused space between the previous track and the newly recorded segment. For lossless linking, it is necessary to write data blocks in the correct position with high accuracy (within 1 micron). For this purpose, the groove is mastered with a high wobble frequency (817kHz), which ensures that the writing can be started and stopped at an accurately defined position. The writing clock as obtained from this groove is very accurate.

ADIP
Address in Pregroove is the name of the process of knowing how far into a disc the laser position is during recording. The Wobbles are counted, and an address location of the section of the disc is calculated.

The CD HF signal path and the DVD signal path needs are different. The DVD signals are handled by the Signal Processor IC for DVD Recording, the SPIDRE. The CD HF signal is handled by the Decoder, IC 7402.

Encoder/Decoder/HDR65

The Encoder/Decoder has the following functions:

- Encoder for DVD+RW. This part creates the EFM+ (16 bit) signals from the I^2S data stream.
- Decoder for DVD and CD. This part processes the HF-signal from the SPIDRE. It converts the EFM(+) signals to data, and performs error detection and error correction.
- Output to SPIDRE pre-processor for RF-AGC.

This IC decodes EFM or EFM+HF signals directly from the SPIDRE. These include: HF, PLL data recovery, demodulation, and error correction.

The Encoder/Decoder has two independent microcontroller interfaces. The first is a serial I^2C bus and the second is a standard 8-bit multiplexed parallel interface. Both of these interfaces provide access to 32k of SRAM 8-bit registers for control and status.

The analog front-end input on Pins 9 and 10 converts the HF input to the digital domain via an 8-bit A/D converter. The A/D is supplied by an AGC circuit to obtain the optimum performance from the converter. An external oscillator is supplied for this subsystem to recover the data from the channel stream. It corrects asymmetry, performs noise filtering and equalization, and finally recovers the bit clock and data from the channel using a digital PLL.

The demodulator portion detects the frame synchronization signals and decodes the EFM (14 bit) and EFM+ (16 bit) data and sub-code words into 8-bit symbols. Via the serial output interface, the I^2S data (audio and video) go to the DVD+RW interface.

The spindle-motor interface provides both motor control signals from the demodulator and, in addition, contains a tachometer loop that accepts tachometer pulses from the motor unit. The motor is a standard three phase motor. Motor speed is controlled by the Wobble Processor during record. During playback, the Wobble processor is monitoring the Data stacked up in the SRAM of 7204. The Motor control signal is on Pin 98 which supplies the drive IC 7301.

AWESOME

AWESOME stands for: Adip decoding, Wobble processing, Error correction, Synchronous start/stop and Occasionally Mend Errors.

The AWESOME gate array chip, IC 7401, is a fully digital DVD+RW add-on for the HDR65. A combination of both ICs can do CD and DVD decoding and CD, DVD-R(W), and DVD+RW encoding. It contains logic for:

- Wobble processing
- Address detection
- Write clock generation
- Start and stop
- ADdress In Pregroove decoding, Adip
- Spindle motor control to do CLV on wobble
- Link bits insertion (according to DVD+RW standard).
- Output to SPIDRE pre-processor for wobble-AGC

It also receives the serial interface signal from the Encoder/Decoder IC on Pins 6, 7, and 8 and merges the internal serial bus to be sent to the analog pre-processor (SPIDRE), on pins 72, 78, and 79.

4 DECODER / ENCODER

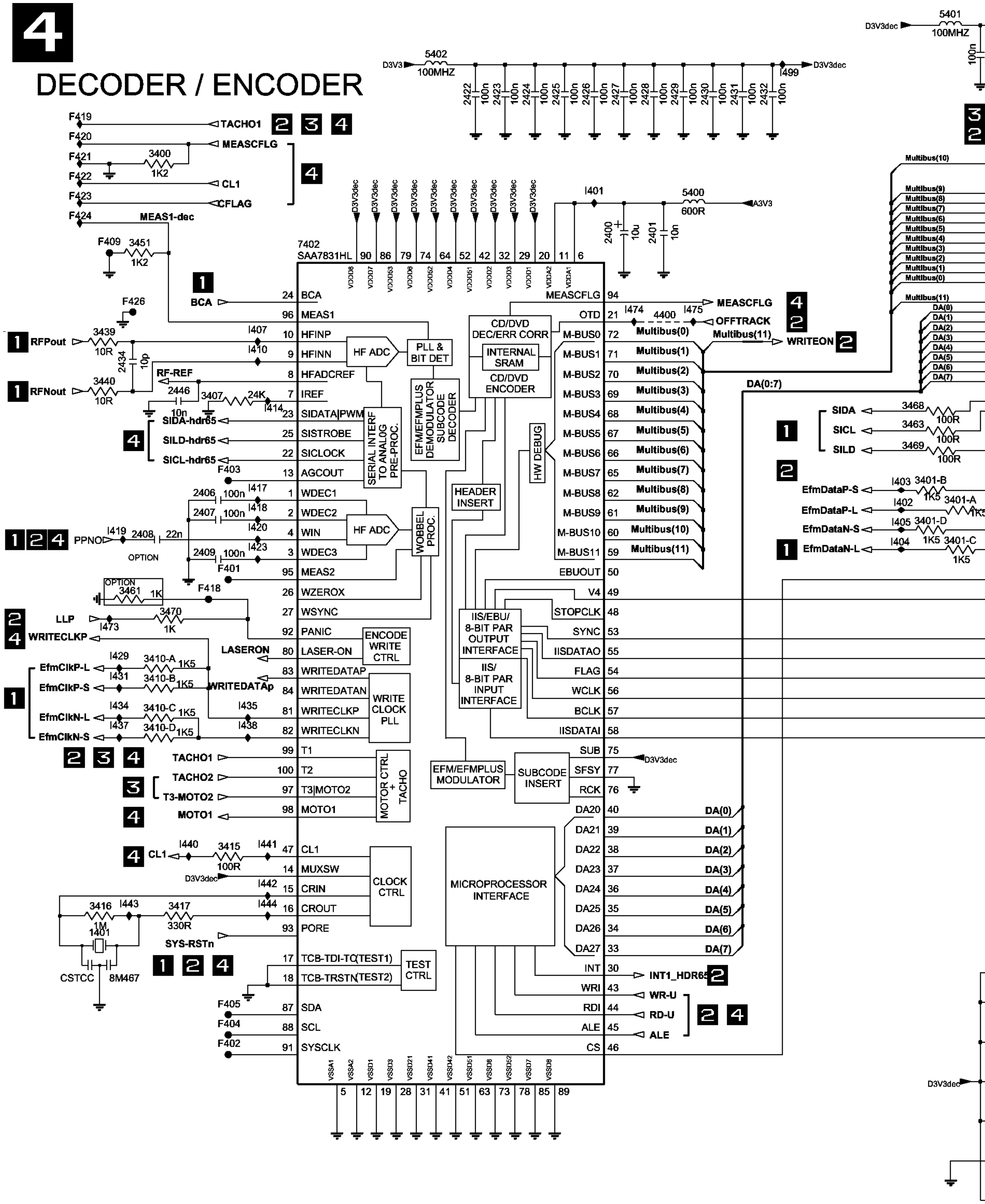
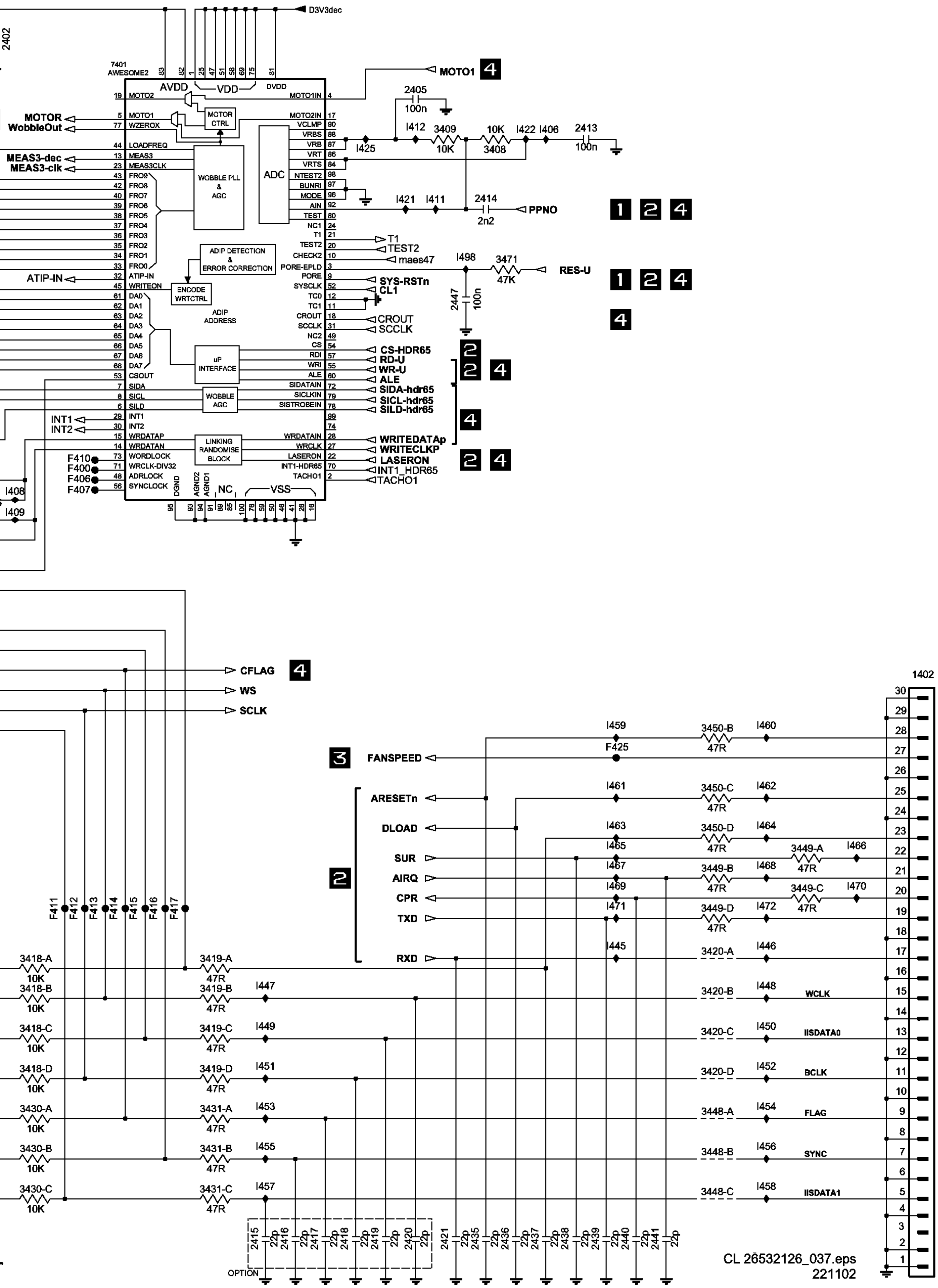


Figure 39 - Encoder/Decoder



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221102

Motor Drivers

The motor drivers each receive an error or control voltage. There are 6 motor drivers in this unit: the Focus Motor Driver, the Radial Motor drivers, the Turntable Motor Driver, the Tilt Motor driver, the Sled motor Driver and the Tray motor Driver.

Focus Motor Driver
The Focus motor is located on the OPU. It controls the up and down motion of the laser's lens. An error signal is produced by the MACE3 Microcomputer. The FO signal comes into Pin 3 of 7302. The Driver circuit amplifies the signal and converts it to a balanced output at Pins 1 and 2 of IC7302. The Output goes to the OPU.

Radial Motor Driver
The Radial motor is located on the OPU. It controls the side to side motion of the laser's lens. This is used in conjunction with the Sled Motor for tracking. An error signal is produced by the MACE3 Microcomputer. The RA signal comes into Pin 25 of 7302. The Driver circuit amplifies the signal and converts it to a balanced output at Pins 26 and 27 of IC7302. The Output goes to the OPU.

Turntable Motor Driver
The Turntable Motor is a standard three phase motor similar to what is found in VCR capstan motor circuits.The driver IC, 7301, receives two control voltages. The Motor Error signal comes into Pin 22. There is a Motor Enable switching voltage coming into Pin 23. A three-phase drive signal is provided to the motor. Three hall elements feed speed and phase data back to the motor driver IC. These signals are amplified. Three FG signals are output to the Encoder/ Decoder from Pins 16, 17, and 18.

Tilt Motor Driver
The Tilt Motor driver contains two signal paths. The motor has two field windings. The Tilt Motor has two error voltages supplied by the MACE3. The Tilt Output Cosine and Tilt Output Sine signals go to Pins 17 and 18 of 7306. The Signals are amplified and provided to the motor on Pins 12-5 of IC7306.

Sled Motor Driver
THe MACE3 produces the SL control voltage for the driver circuit. The Sled motor drive signal is provided to the Sled Motor by 7302. The SL signal comes into IC7302 on Pin 20. A control voltage is developed and amplifiers produce the drive voltages on Pins 17 and 18. These are connected to 1302 on Pins 7 and 8.

Tray motor Driver.
Tray in and Tray out logic control lines are received from the MACE3 and a motor drive signal is provided to the Tray Motor. The logic control signal comes into IC7302 on Pins 15 and 16. A control voltage is developed and amplifiers produce the drive voltages on Pins 12 and 13. These are connected to 1301 on Pins 3 and 4.

3 DRIVER

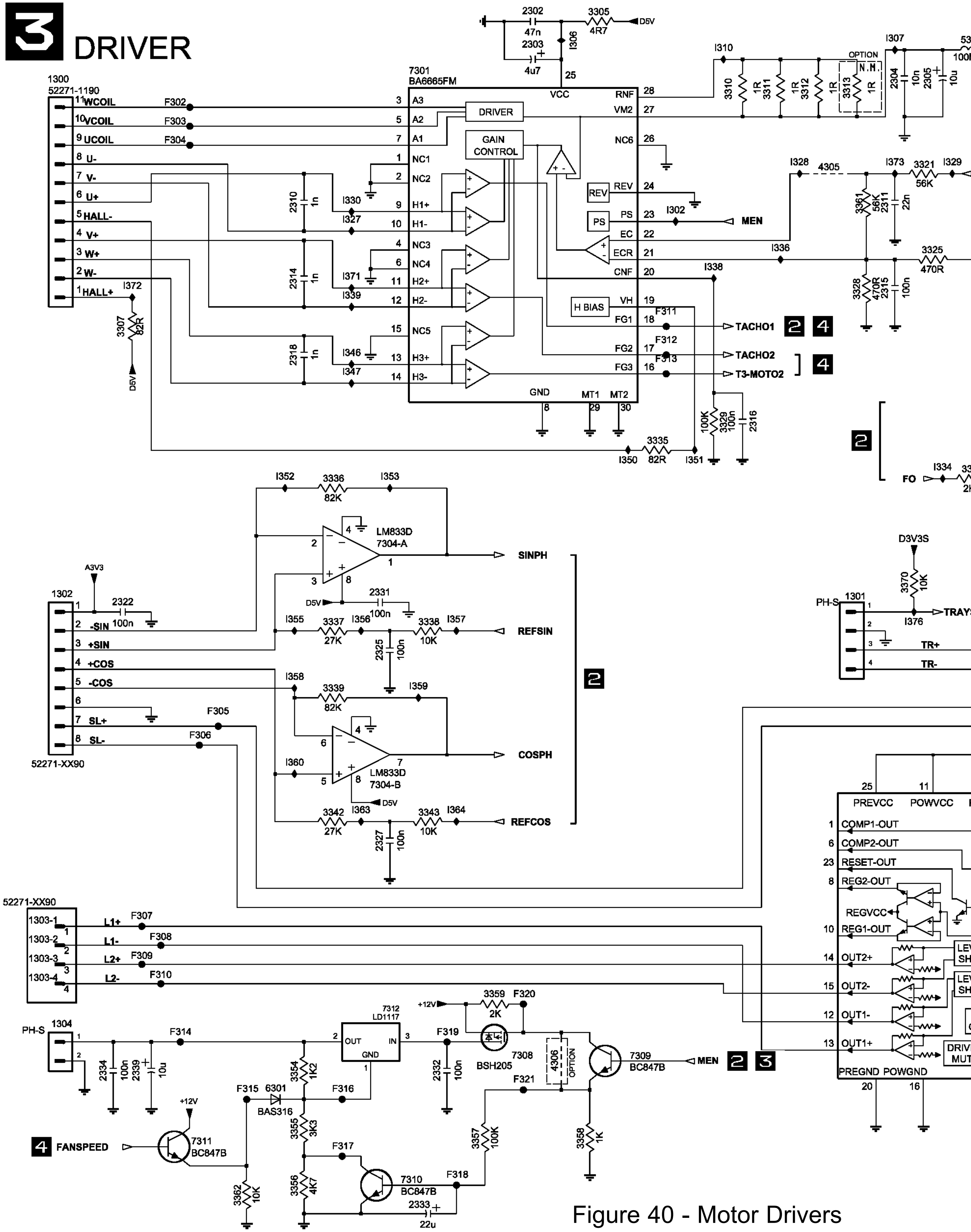
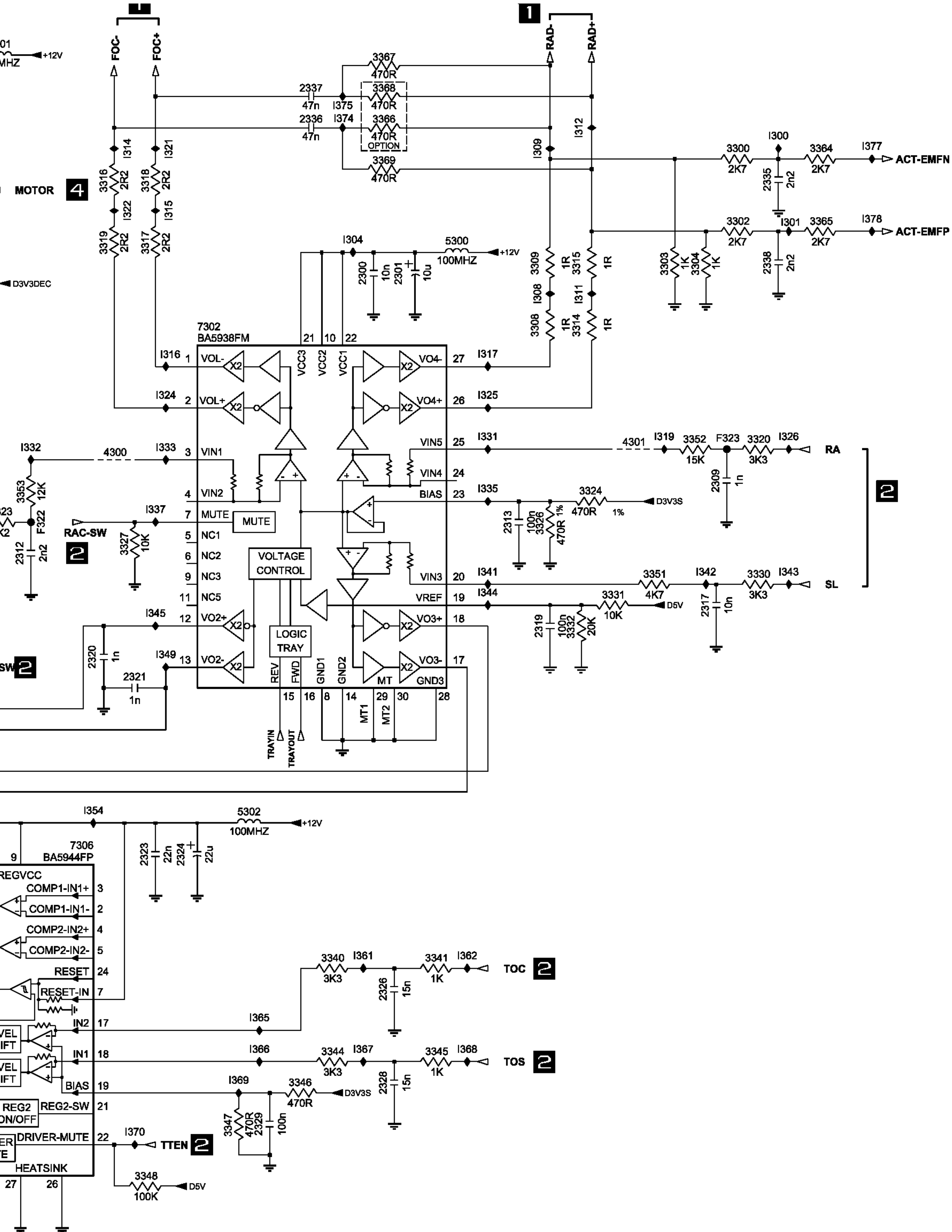


Figure 40 - Motor Drivers



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Troubleshooting

The Power Supply

This Power Supply operates whenever AC power is applied. The primary winding of the transformer operates using Hot Ground. Be sure to use an isolation transformer on the AC input. When working with Switch Mode Power Supplies, there are three general symptoms to be considered: No operation or dead, improper regulation, and one or more supply lines missing.

No Operation
This symptom can be caused by many components. Of course, check the Standby supplies coming from the SMPS. If you can identify a missing supply, then move on to the next section SMPS problems.

When AC is applied to the unit, The System Control Microcomputer Resets and turns On some of the switched supplies, via the STBY control voltage. The 5SW and 8SW supplies are the first group of supplies to be switched On. The Analog Microcomputer Initializes its I^2C bus and communicates with the RF Unit, the Sound IF, the Input Matrix, and the Front Panel. If those circuits operate properly, the ION control voltage goes low to turn On the second set of switched voltages. If the ION switching voltage does not appear, the problem is on the Analog Board or the Front Panel. The Analog Board Microcomputer only allows 10 seconds for this process. and it will only try once.

If the ION switching voltage appears, the Analog Board and the Front Panel are operating well enough to turn On power. The 3.3Vdc is the main supply to most of the microcomputers on many of the PCBs.

VN02 Product

The Analog Board's Microcomputer also sends out the IReset signal to 7902 on the Digital Board. This IC produces a delayed Resetn signal line for the Host Decoder, the VSM, the VIP, and the Line Doubler. The Host Decoder activates the I^2C Bus on the Digital Board. The Host Decoder also produces four reset signals for: the DVIO Board, two of them go to the EMPRESS and one to the VSM. The Digital Board sends a reset to the BE. The Host Decoder expects a response on the I^2C Bus from: the EMPRESS, the VIP, and both Progressive Scan ICs. The BE performs its own reset and self analysis and communicates to the VSM via two signals that it is ready to operate. The SUR line produces a clear to send signal to Pin 24 of the VSM and the PSEN signal must appear. The PSEN signal is 5.3 MHz. If either the SUR line or the PSEN signals do not appear, the VSM will communicate to the Analog Board's Microcomputer, and the Power will be shut down.

If the BE has responded properly and the rest of the Digital Board operates properly, the Host Decoder communicates to the VSM which communicates to System Control Microcomputer on the Analog Board to tell the Front Panel to turn On the Display and wait for customer Keyboard input.

The challenge is to figure out where in this process the machine stops. The Analog Microcomputer allows 10 seconds for the VSM to give the all is well signal. If it does not occur, the ION switching voltage is removed and the unit goes into shutdown.

Listen for the BE reseting the Tilt Motor. It is a vibration noise that is easily heard. The tilt Motor's vibration occurs very near the end of the process. If you can hear it, the Digital Board and Analog Board passed their own initial self test. It also means the BE is nearing the end of its tests. Check for the SUR line coming from the BE to the VSM. If it goes high, the BE has passed its self test and is ready to receive commands from the VSM. There is an ugly squarewave on the SUR line dureing times of communi-

cation. In Powerd Up Standby, the Line is High.
VN04 Product

The focus is going to be proving the problem is on the Digital Board from the inputs and outputs. The main conponent is a 308 pin Ball Grid Array. This makes replacing the Microcomputer very difficult for most servicers. Once you have proven the problem is on the Digital Board, you will probably want to replace the Digital Board.

The ION switching voltage passes through the Digital Board. If the unit is not turning On, this is a good place to start. If it goes Low, The Analog Board and Front Panel have passed their initialization tests.

ION control voltage will only occur once if there is a problem. You must have your meter or scope in place to make the check. The Analog Board only allows 10 seconds for the unit to pass all of its tests. If it does not, it will go into shut down until power is removed.

If the ION control voltage does not go Low, the problem is likely on the Analog or Front Panel Boards. Check for the SCL and SDA on the System Control Microcomputer.

If the ION goes Low for 10 seconds and the unit locks up the unit, the problem could be in the Digital Board. Listen for the BE's Tilt Motor to vibrate. If it does, the Digital Board's Microcomputer and Reset circuits are functional at a basic level. If the BE doesn't vibrate, check the power to the BE and the Digital Board. When ION goes Low all supplies should be available during the 10 second start up process. If the Supplies check out, manually reset the BE by pulling the RESET_BE line Low with a 100 ohm resister. If it still does not vibrate, the problem is in the BE. If it will manually Reset, the problem is on the Digital Board. If the BE vibrates and the unit still shuts down, the problem is likely in the Digital Board, but this is not rock solid. Check for activity on the two UARTS: the one between the BE and the Microcomputer, and the one between the Microcomputer and the System Control Microcomputer on the Analog Board. If UART3 is not proper, the Digital Board is most likely the problem.

SMPS Problems

We are starting with a Dead unit. Connect it to an isolation transformer. Check for 160Vdc on the drain of 7307. If it is not present, there is an open in the AC input circuit. This includes the bridge rectifier and the primary winding of the transformer.

Next, check for voltage on the gate of 7307. It should have about 5 - 6 volts on it. If it is near 0Vdc, check two things. Check the FET for a short. And, check Pin 6 of IC 7313 supplying the gate. If the gate voltage is 4Vdc or more, the FET should be conducting.

Check the voltage on the source. It should be a few tenths at most. If it is higher, replace the source resistors and the FET, 3352, 3321, and 7307. It is a good idea any time the FET is replaced to replace the source resistors. They can read proper and be out of tolerance, causing a repeat failure in a short time.

Is the unit ticking? Place a scope on the drain of the FET. Is there a signal there? If the signal is about 2 Hz, the Overload Circuit may be activating. Remove AC power and check each of the output lines for a short. If no problem can be identified, replace the source sensing resistors, 3321 and 3352. Check Supply AC and monitor Pin 5 of IC 7313. If it reaches .4V, there is an improper load in the circuit or the FET is bad.

Improper Regulation
This type fault will show itself in one of three ways: The outputs are too high, the outputs are too low, or alternate high and low outputs. The precise regulation loop monitors the 5Vdc supply Measure the voltage drop on the diode portion of the optic coupler, 7314.

If the voltages on the output lines are too high, the voltage drop on the diode portion of the optic coupler should be 1-1.2Vdc. The transistor portion should be conducting hard with little or no voltage drop. If there is a voltage drop on the transistor portion, the optic coupler or the drive to it are bad.

If the transistor portion of the optic coupler has little or no voltage drop, the secondary side of the power supply is asking for less output. The problem involves 7313 and associated components. Check 6311. If it is leaky, the sense line will be low in respect to the true output, causing an elevated output. If it is not, the problem replace IC 7313.

If the optic diode has a volt or less, the shunt regulator (7314) and/or the voltage divider resistors can be the problem. Check the diode portion of the optic coupler.

If the voltages on the outputs are too low, the voltage drop on the diode in the optic coupler should be less than a volt. The transistor side should have a 5-6V drop. If these voltages are proper, the secondary portion of the power supply is asking for more output, and the problem is on the primary side.

Check the signal on Pin 5 of 7313. It should be less than .3Vp-p with low output voltages. if its 3. or higher, replace the Sense resistors, 3321 and 3352. If the Sense input is low, IC7313 is likely the problem.

If the diode portion has a volt or more on it, the Shunt Regulator is improperly driving the optic coupler. The problem is with the Shunt Regulator or the voltage dividers.

If the diode portion does not have a voltage drop of .9V or more and the transistor side has a small voltage drop 3V or less, the transistor portion of the optic coupler is faulty.

For a condition of having alternate high and low output voltages, there is a rectification and filtering problem or there is an excessive load on one of the output lines. If there is an excessive load on the 5 Vdc line, the 5V could read normal while the other outputs rise to abnormal levels. The supply is working harder to maintain the 5V on the monitored line but the other outputs receive proportionally more energy. This effect makes their output voltage elevated.

The condition would be very simular if the rectification and filtering were poor on the monitored line.

If the non-monitored line(s) are low, the same two things can happen on just one source. Poor rectification or filtering will cause low output. An excessive load will also cause this symptom.

For a condition of having just one output missing, there is an open in the Rectification/ Filtering circuit. This could include: a fuseable resistor, the winding of the transformer, or problems with the foil pattern on the board. Once the open is identified, measure the line for a short before providing AC to the supply.

The Front Panel/ Display Board

Problems on the Front Panel display fall into four categories: no display function, improper display function, no keyboard function, and no remote control function. Do not consider this board at fault first if all of the symptoms are present. The front panel cannot operate until many functions of self-check pass. A problem on this board more likely shows one of the above symptoms.

The board has several power supply voltages that should be checked first before considering a problem on the board.

No display unit operates
There are three major elements to work with for no display: the fluorescent tube, the Microcontroller and the power supplies dedicated to the tube. The VGNSTBY supply is only used by the tube. Measure the VGNSTBY. It should be -28V or more. If it is not present, trace it back to the power supply. If it is there, check the Filiment supply. It should be 6-8Vac. If it is present, check for the scanning signals on 7103. If they are present the tube is bad. If the scanning signals are missing replace 7103. If the Filiment supply is missing, check for the drive signal from Pin 19 of 7103. If it is present, there is a problem with the drive transistors, 7109, 7108, 7106, and associated components. If the drive is missing, replace 7103.

Improper display
The self diagnostics have a test pattern routine that can help when troubleshooting this type of failure. One of the choices is to light up all of the segments. Set this up to show you what segments are not functioning properly. A pattern should be visible. One row or a column may not be lighting up. Trace out the pin that is responsible for the row or rows that are not lighting. There are diodes connected to these pins. Normally, the diode(s) are bad or there is a foreign substance on the board at that location.

No keyboard function
It takes two Microcomputers to function properly for the keyboard to function: the Microcomputer on the Front Panel, an the microcomputer on the Analog Board, If the display is working, the Front Panel should be showing four dashes. This means the Power up Reset and self check has passed. Check for remote operation. If the remote functions, start with the Analog Board's microcomputer.

Monitor the I^2C Bus while pressing the keyboard. The data should change. If it does, the problem could be on the Digital Board. Check the INT output on Pin 5 of 1910. When a keyboard button is pressed and the Microcomputer reconizes this, the INT line goes low. This communicates to the System Control IC to retreive the data from the Front Panel Microcomputer. If the INT does not go low, the problem is on the Front Panel. If the I^2C bus does not reflect a change in data when a key is pressed, the problem is on the Analog Board. For problems on the Front Panel, check the RTL logic for the keys on the Front Panel. If the Keyboard data seems to be getting into the microcomputer, check the secondary switched supplies. The STBY goes Low to turn on the SW5 and the SW 8Vdc supplies as part of the power up.

No Remote Control Function
It takes two Microcomputers to function properly for the Remote control to function: the Microcomputer on the Front Panel and the microcomputer on the Analog Board. If the display is working, and keyboard function are normal, the Front Panel Microcomputer and the rest of the unit is operating properly. Start with IR receiver's output. The signal should be TTL level. If it is not, be sure the connections are good, supplying the B+ and ground to the Receiver. If the signal is there, check for it on the Front Panel's Microcomputer, Pin 20. If it is missing check 7107 and its support components.

If the signal going to the Front panel Microcomputer is proper, monitor the I^2C Bus

while pressing the remote keyboard. The data should change. If it does not, check all the vitals to the Microcomputer, VCC, grounds, Clocks, and reset the microcomputer as a test. If none of these yield results, suspect the microcomputer.

The Digital Board

The Digital Board is central to the recorder's operation. There are two categories of symptoms that cause the Digital Board to be suspect. One is "No Power" and the other is a more conventional digital signal flow problem. The reason the Digital Board needs to be focused on for a No Power problem is that the Digital Board communicates the condition of the BE and Digital Board to the System Control Microcomputer.

VN02
UART1 of the VSM communicates to the System Control Microcomputer. The Host Decoder IC also produces secondary reset functions for many ICs including the BE. If you are concerned with "No Power" and the SMPS is functioning, go to the No power part of this write up where all the circuits involved in power up will be discussed. For digital signal path troubleshooting, proceed to the next paragraph.

Close scrutiny of the symptom is necessary. If you are considering the problem to be on the Digital Board, you have basic operation of the unit. The unit powers up. The Front Panel's display is proper. The unit will try to play a disc. The symptom involves: no menu, no playback Video or Audio, no record Video or Audio, or scrambled Video or Audio. If you can play a known good disc, you can eliminate half of the circuitry in the Digital Signal Processor. If you see the Video and Audio during the record process, the Digital Board is probably not where your problem is. The parallel loop thru condition that occurs during record utilizes most of the circuitry on the Digital Board and the Analog Board.

If the problem is apparent in playback, use playback for troubleshooting. Use a disc that has colorbars recorded on it. Check the CVBS signal on the output of the Host Decoder. The bars signal allows you to closely scrutinize the signal on the output. If the signal is good, follow the signal through the Analog Board to the output jacks.
If the signal is missing or distorted, scrutinize whether the distortion is caused by digital encodin/decoding or an analog type distortion. Digital problems manifest themselves as blocks or sections of the picure being missing or distored and portions being good. Analog distortions could be smears or loss of detail, loss of color. The Analog Board could be loading the output of the Digital Board. Open the connection to the audio board to separate where the problem is. Un loaded the Video signal should be 2Vp-p. If the problem is on the Digital board. and, the problem is in playback, the problem is likly in the Host decoder or its support circuitry. It receives the Signal directly from the BE and supplies the Video to the Analog Board.

If the unit plays back properly, use the record mode to troubleshoot. Most of the playback circuitry is in operation as well. The output of the VSM supplying the BE is in the middle of the circuitry on the Digital Board. Check the Digital Video stream here. If it is not present, check for it going to the Empress. If it is there, the problem involves the Empress and/or the VSM. If the signal is not present on the inputs to the Empress, check the inputs to the VIP. If the signals are there, stay on the Digital Board, checking for problems with the VIP and/or the Empress. If the signals are not coming into the VIP, the problem is on the Analog Board. For all of these checks you are looking for clean digital transitions of the signal.

VN04

UART3 of the Microcomputer communicates to the System Control Microcomputer. It produces reset for the BE. If you are concerned with "No Power" and the SMPS is functioning, go to the No power part of this write up where all the circuits involved in power up will be discussed. For digital signal path troubleshooting, proceed to the next paragraph.

Close scrutiny of the symptom is necessary. If you are considering the problem to be on the

Digital Board, you have basic operation of the unit. The unit powers up. The Front Panel's display is proper. The unit will try to play a disc. The symptom involves: no menu, no playback Video or Audio, no record Video or Audio, or scrambled Video or Audio. If you can play a known good disc, you can eliminate half of the circuitry in the Digital Signal Processor. If you see the Video and Audio during the record process, the Digital Board is probably not where your problem is. The parallel loop thru condition that occurs during record utilizes most of the circuitry on the Digital Board and the Analog Board.

If the problem is apparent in playback, use playback for troubleshooting. Use a disc that has colorbars recorded on it. Check the CVBS signal on the output on Pin 11 of 1904. The bars signal allows you to closely scrutinize the signal on the output. If the signal is good, follow the signal through the Analog Board to the output jacks. If the signal is missing or distorted, scrutinize whether the distortion is caused by digital encodin/decoding or an analog type distortion. Digital problems manifest themselves as blocks or sections of the picure being missing or distored and portions being good. Analog distortions could be smears or loss of detail, loss of color. The Analog Board could be loading the output of the Digital Board. Open the connection to the Analog Board to separate where the problem is. Unloaded the Video signal should be 2Vp-p. If the problem is on the Digital Board, and the problem is in playback, the problem is likely in the Microcomputer or its support circuitry. It receives the signal directly from the BE and supplies the Video to the Analog Board. Replace the Digital Board.

If the unit plays back properly, and doesn record, the problem is likely on the Digital Board. Replace the Digital Board.

The Analog Board

The Analog Board can display many symptoms. There are three main categories to consider when looking for a problem on the Analog Board: no Power, one or more function inoperative, or a Video/Audio switching problem. If you are working with a No Power problem, go to the No Power portion of this write up. If you are working with a single function that is not operative, trace the control of the function to the System Control IC. For a Video/Audio routing issue, continue with the next paragraph.

It has many inputs and outputs. It contains the Tuner and Modulator functions. It D to A and A to D converts the Audio. Symptoms for this module will be: one or more type of output is missing, or the Tuner does not function properly. Each of the inputs and outputs have separate paths in and out of the module. They all, however, pass through the massive switch, IC7408. The key to an input/output problem will be determining which inputs and outputs are affected. If it is a single signal, follow that line through the circuitry to determine where the signal stops. If more than one signal or all the signals are not passing through the board, 7408 is the place to start.

Tuner problems

This symptom involves two major components, the Tuner and the Demodulator IC7600. Tuner problems fall into two categories: no Tuner function or erratic Tuner function.

No Tuner Functions
As with any circuit, verify the 2 supply voltages. The 33Vdc supply is used exclusively by the Tuner. Check for the presence of the I^2C Bus on the Tuner. This signal controls the operation of the Tuner. If those two conditions are met, there should be video on Pin 24 and IF going to the Sound IF IC. If audio is a problem, provide a substitute IF signal to check the Demodulator IC. If substitution shows the Demodulator is good, replace the Tuner. If no substitution is available, Noise can be introduced into the IF signal path. The Sound IF should amplify noise in the output.

Erratic Tuner Function
Problems described here usually are: the Tuner drifts or won't lock in, certain bands of the Tuner do not function. or, the picture is snowy. Slow

lock in or continuous hunting for lock in is usually internal to the RF Unit. In rare cases, the AFC signal coming from the System Control. It would be rare for the Microcomputer to be the cause. Check the Video input to the Microcomputer. it is probably distorted, causing the Microcomputer to lock in incorrectly.

Audio selection problem.
This type of problem will involve 7501. Check for the control voltages on Pins 9 and 10. Monitor them and select different inputs to be sure they change as you make selections. Check for the output signals on Pins 3 and 13. If they are present check for the serial data coming from the A to D converter. If the signal is at the output the problem is on the Digital Board. If not Check the A/D. Be sure the PWSWON control voltage and supply voltages are present. If they are fine check the incoming clock on Pin 8. If they are present then the IC is bad.

Audio Playback problem
This type problem will also include Power On Standby Audio. Check for the Audio at the input to the Op Amps 7002. If it is present, check for audio on the audio jacks. If it is not there, check for the Mute control voltage on the bases of 7509 and 7511. If there is no signal on the outputs of the Op amps, the Op amps are bad, or the Mute transistors are active or shorted. If the Audio is present on the Outputs, the signal needs to be traced through the Sound IF. The IF selects and combines the audio. Check for the audio on the output of the Sound IF. If it is not here, and all other functions of the Sound IF are working, replace the IC. If it is here, the RF Unit is bad.

Basic Engine

If the PSEN signal is not present, there is a problem in the BE that will interfere with the unit powering up. Other symptom caused by the BE can be playability and recording Problems.

No power up involves the MACE3 Microcomputer. It is the System Control for the BE. Like any microcomputer, first check the supplies, the Oscillator, and the Reset to the IC. Then check for a signal on the SUR line. It Is the Servo Unit Ready. A clear to send clock signal is is seen after the MACE3 checks its memory. After the Tilt Motor vibrates it goes High during Standby. If it doesn't go High, the MACE3, the SRAM, or the Flash Rom are bad. If the MACE oscillator is present, at least part of the chip is functioning. Check for data on the Flash ROM. It is read first. If there is activity, suspect the SRAM. If there is no activity on the FLASH suspect the Flash ROM as bad.

If the Symptom has in the display three words repeating" Opening, Closing, Blocked", the problem is likely the OPU. Those three words could appear when a tray motor problem is occurring, however, the OPU is a much more common occurrence.

There are many symptoms that involve playability, and recordability. Most common is that the unit will not recognize a disk, or a certain type of disk. Sometimes the symptom is that the unit writes or reads for only a few minutes then an error is shown in the display. Another is that the unit has a problem during the Menu update. All of these symptoms and more are usually caused by a bad DVDM.

Edit Problems and Chapter problems have two issues to be resolved. One is the software. There have been many updates to the System software. Many of the updates were designed to fix those kind of issues. FF13g is the current version to be loaded. It is found on update disc version 6.1 If the Software upgrades does not fix the problem, It is likely the OPU is the problem.

List of Abbreviations

1394 IEEE	Serial Digital video and audio transfer protocol
8SC2	Control voltage used by units having a SCART connector. Non U.S.
+12V	+12V Power Supply
+2V5_FLI	+2V5 Power Supply for Line Doubler and SDRAM
+2V5_PLL	+2V5 Power Supply for PLL
+3V3	+3V3 Power Supply
+3V3_ANA	+3V3 Power Supply Analog
+3V3_DD	+3V3 Power Supply Digital
+3V3_DLY	+3V3 Power Supply for IC7500
+3V3_DV	+3V3 Power Supply for IC7404
+3V3_FLI	+3V3 Power Supply for FLI
+3V3_FPGA	+3V3 Internal Power Supply for IC7303
+3V3_FPGA_CONF	+3V3 Power Supply for IC 7300
+3V3_IEEE_A	+3V3 Digital Power Supply for PHY IC 7101
+3V3_IEEE_PLL	+3V3 PLL Power Supply for PHY IC 7101
+3V3_LINK	+3V3 Power Supply IC7103
+3V3_PLL	+3V3 Power Supply IC7307 & IC7308
+3V3_SRAM	+3V3 Power Supply
+3VREG	+3Vdc Standby
+5V	+5V Power Supply
+5V_BUFFER	+5V Power Supply for Video Filters
+5V_PROC	+5V Power Supply IC7200, IC7201, IC7203 & IC7208
+VCC_DV_RAM	+3V3 Power Supply for DV_RAM (IC7400—> IC7404)
1394_RSTN	Reset of LINK IC (7103) and PHY IC (7101)
5508_HS	Horizontal Synchronization from Host Decoder to Progressive Scan
5508_ODD_EVEN	Odd - Even control from Host Decoder to Progressive Scan
-5V	-5V Power Supply
-5V_BUFFER	-5V Power Supply for Video Filters
+35V_DV_EDO	+3V3 Power Supply EDO Bus IC7404 A (0:8) Address lines
A1, A2	Power Calibration maximum and Minimum signals
A_EMPRESS (13:0)	EMPRESS Address Output to SDRAM
A_YCVBS	Selected Luminance or Composite Video sent to the Digital Board
ACC_ACLK_OSC	Audio Clock PLL Output syncronized with incoming Video for record
ACC_ACLK_PLL	Audio Clock PLL Output for play back
ACLK_EMP	EMPRESS Audio Clock Output
AD_ACLK	Audio Decoder Clock
AD_BCLK	Audio Decoder I^2S bit Clock
AD_DATAO	Audio Decoder Output Data (PCM)
AD_SPDIF33	Audio Digital Output to the Analog Board
AD_WCLK	Audio Decoder I^2S Word Clock
ADIP	Address in Pregroove
ADC	Analog to Digital Conversion
AE_ACLK	Audio Encoder Clock
AE_ACLK_OEN	Audio Encoder Clock Output Enable
AE_BCLK	Audio Encoder I^2S bit Clock

AE_BCLK_DV	Audio Encoder I^2S bit Clock to DVIO
AE_BCLK_VSM	Audio Encoder I^2S bit Clock to VSM
AE_DATAI	Audio Encoder Input Data (PCM)
AE_DATAI_DV	Audio Encoder Input Data (PCM) from DVIO
AE_DATAO	Audio Encoder Output Data (PCM)
AE_WCLK	Audio Encoder I^2S Word Clock
AE_WCLK_DV	Audio Encoder I^2S Word Clock to DVIO
AE_WCLK_VSM	Audio Encoder I^2S Word Clock to VSM
ANA_WE	Analog Write Enable Decoder
ANA_WE_LV	Analog Write Enable Low Voltage
AUD_BCLK	Audio Bit Clock
AUD_MUTE	Audio Mute
AUD_SDI	Audio Serial Data Input
AUD_SDO_CON	Audio Serial Data Output to buffer IC 7505
AUD_SDO_DAC	Audio Serial Data Output to DAC IC 7506
AUD_WS_701	Audio Word Select to DV CODEC IC 7404
AUD_WS_OUT	Audio Word Select to buffer IC 7505
AFCLI	Audio from the Front connector Left Input
AFCRI	Audio from the Front connector Right Input
AFEL	Audio from the Front End Left
AFER	Audio from the Front End Right
AINFL	Audio In Front Left
AINFR	Audio In Front Right
AKILL	Control voltage for Mute circuit
ALADC	Audio Left from the Analog to Digital Converter
ALDAC	Audio Left from the Digital to Analog Converter
AMCO	Audio to the RF Modulator Combined Output
ARADC	Audio Right from the Analog to Digital Converter
ARDAC	Audio Right from the Digital to Analog Converter
ASC1M	Control voltage used by units having a SCART connector. Non U.S.
AWSOME	Adip decoding Wobble processing Error correction Synchronous start/stop and Occasionally Mend Errors
B_IN_VIP	Video Blue Input to Video Input Processor
B_OUT	Video Blue Output from Host
B_OUT_B	Buffered Blue Video Output
BA	Bank Address
BCLK_CTL_SERVICE	Bitclock control Service Interface
BE_BCLK	Basic Engine I^2S bit Clock
BE_BCLK_VSM	Basic Engine I^2S bit Clock to VSM
BE_CPR	Basic Engine Control Processor ready to accept Data
BE_DATA_RD	Basic Engine Data Read
BE_DATA_WR	Basic Engine Data Write
BE_FAN	Basic Engine FAN
BE_FLAG	Basic Engine error Flag
BE_IRQN	Basic Engine interrupt request
BE_LOADN	Basic Engine LOAD (LOW active)
BE_RXD	Basic Engine S2B received Data
BE_SUR	Basic Engine Servo Unit Ready to accept Data (S2B)

BE_SYNC	Basic Engine sector/abs time Sync
BE_TXD	Basic Engine S2B transmitted Data
BE_V4	Basic Engine versatile Input pin
BE_WCLK	Basic Engine I^2S Word Clock
BE	Basic Engine/Mechanism-Servo Board
BUFENN_AUD	Buffer Enable Audio
BUFENN_VID	Buffer Enable Video
C_IN	Video Chrominance Input
C_IN_VIP	Chrominance Input to Video Input Processor
C_OUT	Chrominance Output from Host Decoder
C_OUT_B	Filtered Chrominance Output
CALF	Laser Calibration Final voltage
CAS	Column Address strobe
CAV	Constant Angular Velocity
CB_OUT (9:0)	Digital Chrominance Blue Out. One of Y, Cr/Cb
CCIR656	Serial Digital Video transfer Protocol. It is widely used having many resolutions
CCLK	Configuration Clock
CFIN	Chrominance Front Input signal
Cinch	Standard Video and Audio connector
CLK4	SDRAM Clock
CLK27M	27MHz Clock
CLK27M_CON	27MHz Clock to Digital Board
CLK27M_DV	27MHz Clock Digital Video Codec
CLK27M_OSC\	27MHz Clock IC7304
CLOCKGENAUD	Clock generator Audio
CLOCKGENVID	Clock generator Video
CLV	Constant Linear Velocity
ComPair	Computer aided rePair
Cosphi	Cosine Position of Hall info
CPUINT0	Control Processor Unit Interrupt
CPUINT1	Control Processor Unit Interrupt
CPR	Control Processor Ready
CR_OUT (9:0)	Digital Chrominance Red Out. One of Y, Cr/Cb
CS	Chip Select
CSW_SWW	Channel Select Switch control voltage
CTS1P	Clear to send (Service Interface)
CTSN	Clear to Send
CVBR	CD Variable Bit Rate recording
CVBS_OUT	Composite Video Output out of the Host Decoder
CVBS_OUT_B	Buffered Composite Video Output
CVBS_OUT_B_VIP	Composite Video to Video Input Processor (Digital Board Video loop)
CVBS_Y_IN	Composite Video/Luminance Input
CVBS_Y_IN_A	Composite Video/Luminance Input to Video Input Processor
CVBS_Y_IN_B	Composite Video/Luminance Input to Video Input Processor
CVBS_Y_IN_C	Composite Video/Luminance Input to Video Input Processor
CVBSFIN	Composite video Front Input signal.
D_ADDR (10:0)	Address bus
D_CVBS	Composite Video coming from the Digital Board

D_DATA (29:0)	Data bus
D_EMPRESS (15:0)	SDRAM Data Input/Output of EMPRESS
D_PAR_D (7:0)	Front-end parallel interface Data (record)
D_PAR_DVALID	Front-end parallel interface Data valid
D_PAR_REQ	Front-end parallel interface request
D_PAR_STR	Front-end parallel interface strobe
D_PAR_SYNC	Front-end parallel interface Sync
DAC	Digital to Analog Converter
DAIO	Digital Audio Input/Output
DAOUT	Digital Audio Out
DATA	Data from config ROM
Deinterlacer	Converts interlaced video to progressive scan. Line Doubler
DENC	Digital Encoder
DFU	Direction For Use: description for the end user
DNR	Dynamic Noise Reduction
DONE	Indication of the completion of the configuration process
DOUT	Serial configuration Data Output
DRAM	Dynamic RAM
DROPPI	DVD Rewriteable OPU Pre-Processor IC
DSD	Direct Stream Digital
DSP	Digital Signal Processor
DV_ASN	DVCODEC Address Strobe
DV_DRQN	DVCODEC Data Request Interrupt
DV_DSLN	DVCODEC Data Strobe Lower 8 bits
DV_DSUN	DVCODEC Data Strobe Upper 8 Bits
DV_DTACKN	Data Transfer Acknowledge
DV_ERRN	DVCODEC Error Interrupt
DV_HS_IN	DVCODEC Horizontal synchronization In
DV_HS_OUT	DVCODEC Horizontal synchronization Out
DV_IN_CLK	Digital Video IN Clock from DVIO Board
DV_IN_DATA (7:0)	Digital Video IN Data bus from DVIO Board
DV_IN_HS	Digital Video IN Horizontal Synchronization from DVIO Board
DV_IN_VS	Digital Video IN Vertical Synchronization from DVIO Board
DV_LCN	DVCODEC Last Code Interrupt
DV_PDN	DVCODEC Power Down
DV_RSTN	DVCODEC System Reset for NW701
DV_RWN	DVCODEC Read/Write control signal
DV_VS	DVCODEC Vertical synchronization
DVCODEC	Digital Video enCODing and DECoding protocol.
EFM	Eight to Fourteen bit Modulation
EMI_A (21:1)	External Memory Interface Address Bus (Host Decoder)
EMI_BE0N	External Memory Interface Lower byte Enable (Host Decoder)
EMI_BE1N	External Memory Interface Upper byte Enable (Host Decoder)
EMI_CAS0N	External Memory Interface SDRAM column Address strobe
EMI_CE1N	External Memory Interface VSM Lower bank Enable
EMI_CE2N	External Memory Interface VSM Higher bank Enable
EMI_CE3N	External Memory Interface flash IC's Enable
EMI_D (15:0)	External Memory Interface Data Bus (Host Decoder)
EMI_PROCCLK	External Memory Interface Processor Clock (Host Decoder)
EMI_RAS1n	External Memory Interface Row Addres Strobe bank 1

EMI_RWN	External Memory Interface Read/Write control signal (Host Decoder)
EMI_WAIT	External Memory Interface Wait state request (Host Decoder)
EMPRESS_BOOT	EMPRESS BOOT select Input
EMPRESS_IRQN	EMPRESS Interrupt request Output
EPG	Electronic Program Guide
FBIN	Fast Blanking IN. Used by units having a SCART connector.
FDS	Full Diagnostic Software
FIFO	First In First Out memory
FIFOA_A (0:15)	FIFO buffer A Address bus
FIFOA_OEN	FIFO buffer A Output Enable
FIFOA_WEN	FIFO buffer A Write Enable
FIL1	Filiment supply
FIL2	Filiment supply
FLASH_OEN	FLASH Output Enable control signal
FOME	FOllow ME. Used in units having a SCART connector.
FPGA	Field Programmable Gate Array
FTC	Fast Track Count
G_IN_VIP	Video green Input to Video Input Processor
G_OUT	Video green Output from Host Decoder
G_OUT_B	Buffered Green Video Output from Host Decoder
GNDD	Digital signal Ground
HD_M_AD (13:0)	Host Decoder SDRAM Address bus
HD_M_CASN	Host Decoder SDRAM column Address strobe
HD_M_CLK	Host Decoder SDRAM Clock
HD_M_CS0N	Host Decoder SDRAM chip select
HD_M_DQ (15:0)	Host Decoder SDRAM Data bus
HD_M_DQML	Host Decoder SDRAM Data mask Enable (Lower)
HD_M_DQMU	Host Decoder SDRAM Data mask Enable (Upper)
HD_M_RASN	Host Decoder SDRAM row Address strobe
HD_M_WEN	Host Decoder SDRAM write Enable
HF	High Frequency/signal from the disc
HSOUT	Horizontal synchronization OUT
I^2C	Serial communication protocol
I^2S	Integrated IC Sound Buss (3.3V High)
INITN	Initiate Configuration
INT	Interupt - Front Panel Microcomputer signifying to System Control Microcomputer keyboard input data received
IO (0:30)	Data bus of IC7404
IOE	Input Output Extention only used in certain models
ION	Inverted ON: Enable the power Supply for the Digital Board when LOW
IPFAIL	Interupted Power Failure response signal
IPOR	Inverted Power On Reset
IRESET_DIG	Initialization of the Digital Board, HIGH when power ON
ISPN	In System Program Line (used for programming IC7203)
JTAG3_TCK	JTAG Test Clock
JTAG3_TD_VIP_TO_VE	JTAG Transmitted Data Video Input Processor to Video Encoder
JTAG3_TD_VSM_TO_VIP	JTAG Transmitted Data Versatile Stream Manager to Video Input

	Processor
JTAG3_TMS	JTAG Test Mode Select
JTAG3_TRSTN	JTAG Test part ResetN
LADIC	LAser Drive IC
LCASN	Lower Column Address strobe for IC7404 DRAMS
LDON	Laser Drive On
LEVELSW	Control Voltage used in units having a SCART connector.
Line Doubler	Converts Interlace Scan, NTSC, to Progressive Scan
LINK_AVCLKLINK IC	Audio/Video Interface Clock
LINK_AVFSYNC	LINK IC Audio/Video frame Sync
LINK_AVREADY	LINK IC Audio/Video Data ready to send
LINK_AVSYNC	LINK IC Audio/Video packet Sync
LINK_AVVALID	LINK IC Audio/Video Data valid
LINK_CSN	LINK IC chip select
LINK_INTN	LINK IC interrupt
LINKFIFO_DQ (0:7)	Audio Video Data interface
LLD	Loss Less Decoder
LLP	Laser Low Power
LOAD_DVN	LOAD Digital Video (LOW active)
LPCM	Linear Pulse Code Modulation
LRCLK	Left/Right Clock
MACE	Mini All CD Engine
Mpeg	Motion Picture Experts Group (compression scheme)
MUTEN	Mute Enable
MUTEN_LV	Mute Enable Low Voltage
NVM	Non Volatile Memory
OPC	Optimum Power Cailibration
ORD	Radial Drive disable
OPU	Optical Pickup Unit
P_SCAN_YUV (7:0)	Progressive Scan Digital Video bus
P50	Control Voltage used in units having a SCART connector.
PA (0:15)	SRAM processor Address
PCS	Position Control Sled
PCM	Pulse Code Modulation
POR_DC	Power On Reset
PPN	Wobble Pre-Processor signal
PPNO	Wobble Pre-Processor signal Output signal
PWRN	Processor write
SYSCLK_VSM_5508	System Clock VSM and Host decoder
PAD (0:7)	SRAM processor Data
PALE	Processor Address Latch Enable
PHY_CAN	PHY 1394 cable not active
PHY_LPS	LINK IC power status
PINT0N	Processor interrupt 0
PINT1N	Processor interrupt 1
PRDN	Processor read
PROGRAMN	Low active Input to initiate a configuration cycle
PRSTN	Processor reset
R_IN_VIP	Video Red Input to Video Input Processor
R_OUT	Video Red Output from Host Decoder

R_OUT_B	Buffered Red Video Output from Host Decoder
RAS	Row Address Strobe
RASN	Row Address strobe Enable
Refsin	Reference voltage for Hall sensor amp
Refcos	Reference voltage for Hall sensor amp
RESETN	Reset Host Decoder, VSM, and DENC
RESETN_BE	System reset basic engine (buffered)
RESETN_DVIO	System reset Digital Video Input Output (buffered)
RESETN_VE	System reset Video Encoder
ROMH_CEN	Flash 2 chip Enable
ROML_CEN	Flash 1 chip Enable
RSA1	Control voltage for Audio input selection
RSA2	Control voltage for Audio input selection
RSTN_BE	Reset control of basic engine
RSTN_DVIO	Reset control of DVIO
RSTAT	Status Read
RTS1P	Ready To Send Data to service serial interface
RTSN	System Reset
RXD	Receive Data
RX1P	Receive Data from service serial interface
S2B	Serial to Basic Engine Communication
SCL	I^2C bus Clock
SCLSW	I^2C bus Clock with its dc level switched
SD_CASN	SDRAM Column Address strobe Output (active LOW)
SD_CLK	SDRAM Clock Output
SD_CLKE	SDRAM Clock Enable Output
SD_CSN	SDRAM Chip Select
SD_DQM (1:0)	SDRAM Data mask Enable Output
SD_RASN	SDRAM Row Address strobe Output
SD_WEN	SDRAM Write Enable Output
SDA	I^2C bus Data
SDASW	I^2C bus Data with its dc level switched
SEL_ACLK1	Select Audio Clock (playback)
SDRAM	Synchronous DRAM
Sinphi	Sine Position of Hall info
SM_CS3N	SRAM chip select
SM_LBN	SRAM lower bank strobe
SM_OEN	SRAM Output Enable
SM_UBN	SRAM upper bank
SM_WEN	SRAM write Enable
SMA (17:0)	SRAM Address Output
SMD (15:0)	SRAM Data Input/Output
SPDIF	Sony Philips Digital Interface for Audio
SPIDRE	Signal Processing IC for DVD REwritable
SRAM	Static Random Access Memory
SRAMCE0N	SRAM processor chip Enable 0
SRAMRDN	SRAM processor Output Enable
STBY	Control voltage Turns On the 5SW and 8SW supplies

SVCD	Super Video CD
Subcode	Tacking information/Track number/and disc location information
SYSCLK_EMPRESS	System Clock EMPRESS
SYSCLK_PROGSCAN	System Clock Progressive Scan
SYSCLK_VSM_5588	System Clock for the VSM and the Host Decoder
TCK	Boundary scan Test Clock
Temp Sensor	Temperature sensor's output signal
TDI	Boundary scan Test Data Input
TDO	Boundary scan Test Data Output
TDO_CONF	Boundary scan Test Data Output from IC 7309
TLL	Track Loss signal
TMS	Boundary scan Test Mode Select
TPI	Track Position Indicator
TX1P	Transmit Data to service serial interface
TXD	Transmitted Data
U_IN	Video U Input
U_IN_VIP	Video U Input to Video Input Processor
UCASN	Upper column Address
V_IN	Chrominance V Input
V_IN_VIP	Chrominance V Input to Video Input Processor
VBR	Variable Bit Rate recording
VCC3_CLK_BUF	Power Supply 3V3 Clock buffer
VCC3_VSM	Power Supply 3V3 Versatile Stream Manager
VCC3_VSM_MEM	Power Supply 3V3 Versatile Stream Manager Memory
VCC5_4046	Power Supply 5V to PLL IC
VDD_125	Power Supply 5V to buffer 7202
VDD_CORE	Sti5508 Core Supply voltage 2.5V
VDD_EMP	Empress Supply voltage 3.3V
VDD_EMP_CORE	Empress Core Supply voltage 2.5V
VDD_FLASH_H	Flash 7301 Supply voltage
VDD_FLASH_L	Flash 7302 Supply voltage
VDD_LVC32	Power Supply LVC32
VDD_PCM	Power Supply Audio decoder of Sti5508
VDD_PLL	Power Supply PLL Audio decoder of Sti5508
VDD_RGB	Power Supply Video encoder of Sti5508
VDD_STI	Power Supply of Sti5508 and SDRAM
VDD_YCC	Power Supply Video encoder of Sti5508
VDD5_MK2703	Power Supply MK2703
VDD5_OSC	Power Supply Oscillator
VDDA1A_7118	Power Supply for Analog Input of VIP
VDDA2A_7118	Power Supply for Analog Input of VIP
VDDA3A_7118	Power Supply for Analog Input of VIP
VDDA4A_7118	Power Supply for Analog Input of VIP
VDDE_7118	Power Supply Digital for peripheral cells of VIP
VDDI_7118	Power Supply Digital for core of VIP
VDDX_7118	Power Supply for crystal oscillator of VIP
VE_DATA (7:0)	Video Encoder Data Bus
VE_DSn	Video Encoder Data Strobe
VE_DTACKn	Video Encoder Data Transfer acknowledge
VGNSTBY	Negative Supply for the Grids of the Flouresent display

Written by Dan Crum
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